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RENESAS

User's Manual

μPD7755 FAMILY

SPEECH SYNTHESIZER LSIs

μPD7755
μPD7756A
μPD77P56
μPD7757
μPD7758A
μPD7759

Document No. S13148EJ5V0UM00 (5th edition)
(Former Document No.IEU-1218)
Date Published November 1997 N

Phase-out/Discontinued

[MEMO]

SUMMARY OF CONTENTS

Phase-out/Discontinued

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

Phase-out/Discontinued

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Main Revisions in This Edition

Page	Description
Throughout the manual	Addition of the devices shown below. • μPD7755GT-XXX • μPD7756AGT-XXX • μPD7757GT-XXX • μPD7758AGT-XXX
p.12,p.14,p.17,p.34	Addition of descriptions about external clock in **CHAPTER 2 PIN FUNCTIONS** and **3.5 Clock Generator.**
p.43, p.58	Change of the devices which are used in **CHAPTER 4 APPLICATION CIRCUIT EXAMPLES.** • μPD70008 → μPD78001B • μPC1213 → μPC1316

The mark ★ shows revised points.

PREFACE

Target: This manual is intended for the user engineer who intend to understand the μPD7755 family function and design application systems using the μPD7755 family.

μPD7755 family LSI;
- μPD7755
- μPD7756A
- μPD77P56
- μPD7757
- μPD7758A
- μPD7759

Purpose: The purpose of the manual is for the user to understand the μPD7755 family hardware function listed as follows.

- Introduction
- Pin functions
- Operation overview
- Application circuit examples

Use: The manual assumes that the reader has general knowledge of electronics, logical circuit, and speech synthesizer LSI.

Legend:

Data weight	. . . .	High-order and low-order are indicated from left to right
Active low	. . . .	$\overline{xxx}$ (pin or signal name is overlined)
Memory map address	. . . .	Upper stage-low order, lower stage-high order
Note	. . . .	Explanation of (Note) in the text.
Caution	. . . .	Caution to which you should pay attention.
Remarks	. . . .	Supplementary explanation to the text.
Number	. . . .	Decimal number — xxxx Hexadecimal number — xxxxH

Related documents: Use also the following documents.

For Devices

- Data sheet
  - μPD7755, 7756A, 7757, 7758A Data Sheet (IC-2254)
  - μPD77P56 Data Sheet (IC-2324)
  - μPD7759 Data Sheet (IC-2323)
- User's Manual
  - μPD7755 Family User's Manual (This Manual)
- Pamphlet
  - SPD Speech Processing Device (IF-1034)

For Support tools

- User's Manual
  - NV-300 System Speech Analysis Tool
    for μPD7755 Family User's Manual (EEP—1023)

- NV-310 System Speech Emulation Tool
  for μPD7755 Family User's Manual (EEU-1359)

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CONTENTS OF FIGURES (1/2)

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CONTENTS OF TABLES

[MEMO]

CHAPTER 1 INTRODUCTION

μPD7755, 7756A, 77P56, 7757, 7758A, and 7759 are fixed-word speech synthesizer LSIs that operate on the ADPCM (Adaptive Differential Pulse Code Modulation) method basically. They are generically called the μPD7755 family.

The μPD7755 family adopts two methods of speech synthesis, which are applied to various types of speech application systems.

(1) ADPCM method . . . . suitable for clear and natural speech sounds (especially voice and word).
(2) PCM + waveform element method . . . . suitable for various melodies and sound effects.

The further compression coding of the ordinary PCM data is done by the above-mentioned two methods in accordance with each suitable synthesis sound. Therefore the data can be synthesized longer than the ordinary PCM data at the same ROM size.

By using those methods together, the μPD7755 family realize the long-time synthesis of high-quality sounds.

- μPD7755, 7756A, 7757, and 7758A have internal mask ROMs as speech data memory, so they are suitable for integration in compact devices. Each on-chip ROM size is as follows:
  - μPD7755 . . . . 96 Kbits
  - μPD7756A . . . 256 Kbits
  - μPD7757 . . . . 512 Kbits
  - μPD7758A . . . 1 Mbits
- μPD77P56 has internal 256 Kbits one-time PROM, which the user can write speech data in. So the μPD77P56 is suitable for evaluation of applications during system development and also small-volume production.
- μPD7759 is an external ROM type, and speech data memory (ROM: up to 1 Mbits) can be connected externally. The μPD7759 allows the synthesis of speech sounds of any length by using the ADPCM data transferred from an external devices. Therefore, the μPD7759 is suitable for use in devices requiring longer period of speech synthesis and in equipments produced in relatively small volumes.

Phase-out/Discontinued

1.1 μPD7755 Family Features

NEC Speech Synthesizer LSI Family

Item \ Device		μPD7755	μPD7756A	μPD7757	μPD7758A	μPD77P56	μPD7759
Synthesis method		ADPCM, PCM + waveform element					
Sampling frequency		5, 6, 8 kHz					
Speech data memory		96 Kbits mask ROM	256 Kbits mask ROM	512 Kbits mask ROM	1 Mbits mask ROM	256 Kbits one time PROM	1 Mbits external memory
Synthesizing time	Speech[Note] (ADPCM)	4 sec (TYP.)	12 sec (TYP.)	24 sec (TYP.)	50 sec (TYP.)	12 sec (TYP.)	50 sec (TYP.)
	Melodies & sound effects (PCM + waveform element)	30 sec (TYP.)	85 sec (TYP.)	170 sec (TYP.)	340 sec (TYP.)	85 sec (TYP.)	340 sec (TYP.)
★ Package		• 18-pin plastic DIP (300 mil) • 24-pin plastic SOP (450 mil) • 24-pin plastic SOP (375 mil)				• 20-pin plastic DIP (300 mil) • 24-pin plastic SOP (450 mil)	• 40-pin plastic DIP (600 mil) • 52-pin plastic QFP (□14 mm)

Note The speech synthesizing time for the speech (voice, word) at a 6 kHz Sampling. And the speech synthesizing time varies greatly depending on the sampling frequency.

Phase-out/Discontinued

1.2 Ordering Information

Part Number	Package	Quality Grade	
μPD7755C-XXX	18-pin plastic DIP (300 mil)	Standard	
μPD7755G-XXX	24-pin plastic SOP (450 mil)	Standard	
μPD7755GT-XXX[Note]	24-pin plastic SOP (375 mil)	Standard	★
μPD7756AC-XXX	18-pin plastic DIP (300 mil)	Standard	
μPD7756AG-XXX	24-pin plastic SOP (450 mil)	Standard	
μPD7756AGT-XXX	24-pin plastic SOP (375 mil)	Standard	★
μPD77P56CR	20-pin plastic DIP (300 mil)	Standard	
μPD77P56G	24-pin plastic SOP (450 mil)	Standard	
μPD7757C-XXX	18-pin plastic DIP (300 mil)	Standard	
μPD7757G-XXX	24-pin plastic SOP (450 mil)	Standard	
μPD7757GT-XXX[Note]	24-pin plastic SOP (375 mil)	Standard	★
μPD7758ACR-XXX	18-pin plastic DIP (300 mil)	Standard	
μPD7758AG-XXX	24-pin plastic SOP (450 mil)	Standard	
μPD7758AGT-XXX[Note]	24-pin plastic SOP (375 mil)	Standard	★
μPD7759C	40-pin plastic DIP (600 mil)	Standard	
μPD7759GC-3BH	52-pin plastic QFP (□14 mm)	Standard	

Note Under development

Remark xxx is the ROM code specification number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

1.3 Internal Block Diagrams

Fig. 1-1 is an internal block diagram of μPD7755, 7756A, 7757, and 7758A. Fig. 1-2 is an internal block diagram of μPD77P56. Fig. 1-3 is an internal block diagram of μPD7759.

Fig. 1-1 μPD7755, 7756A, 7757, and 7758A internal block diagram

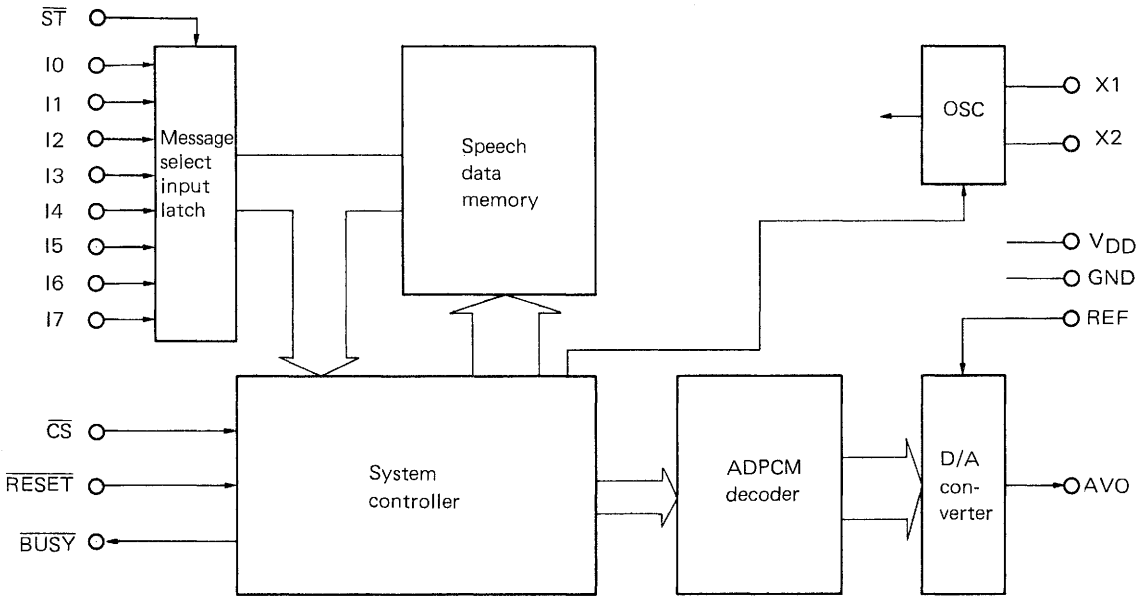


Fig. 1-2 μPD77P56 internal block diagram

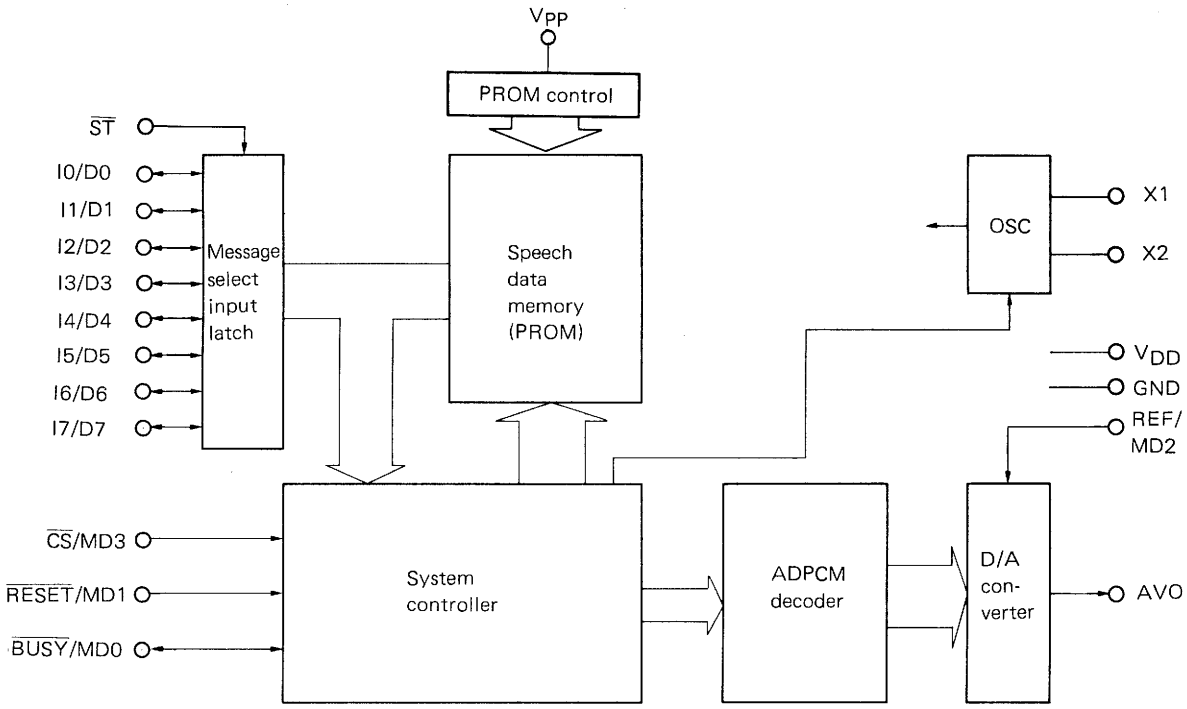
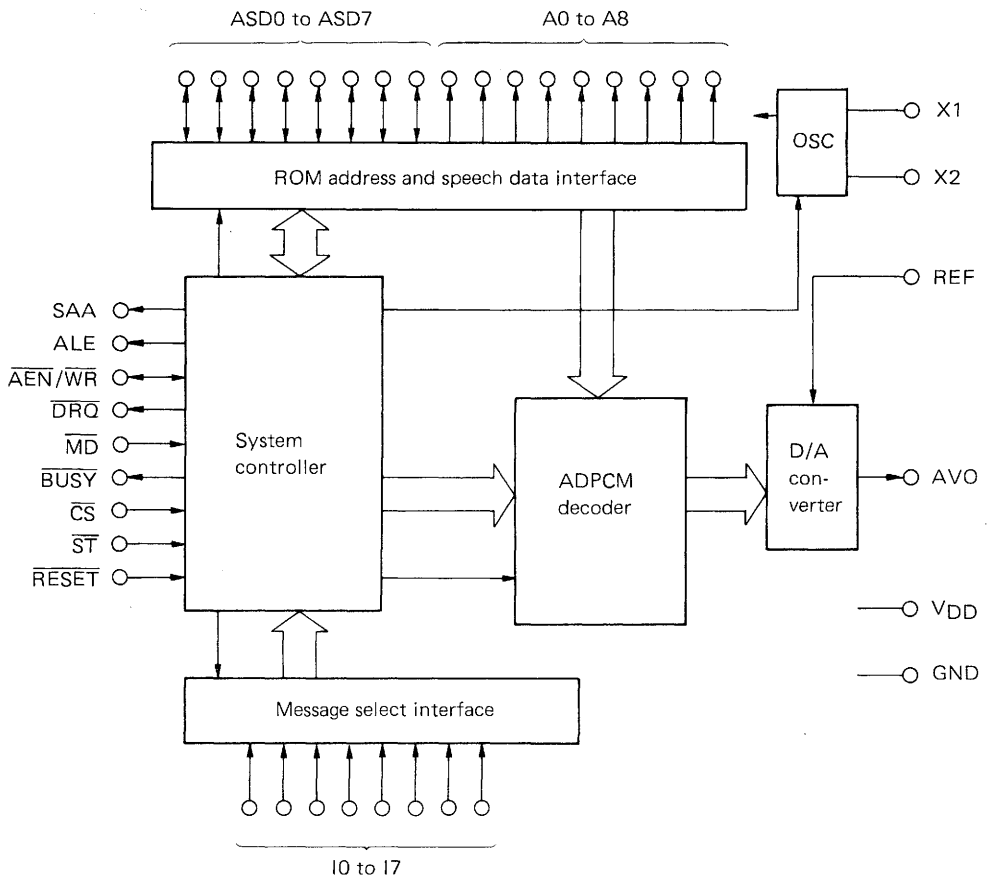


Fig. 1-3 μPD7759 internal block diagram



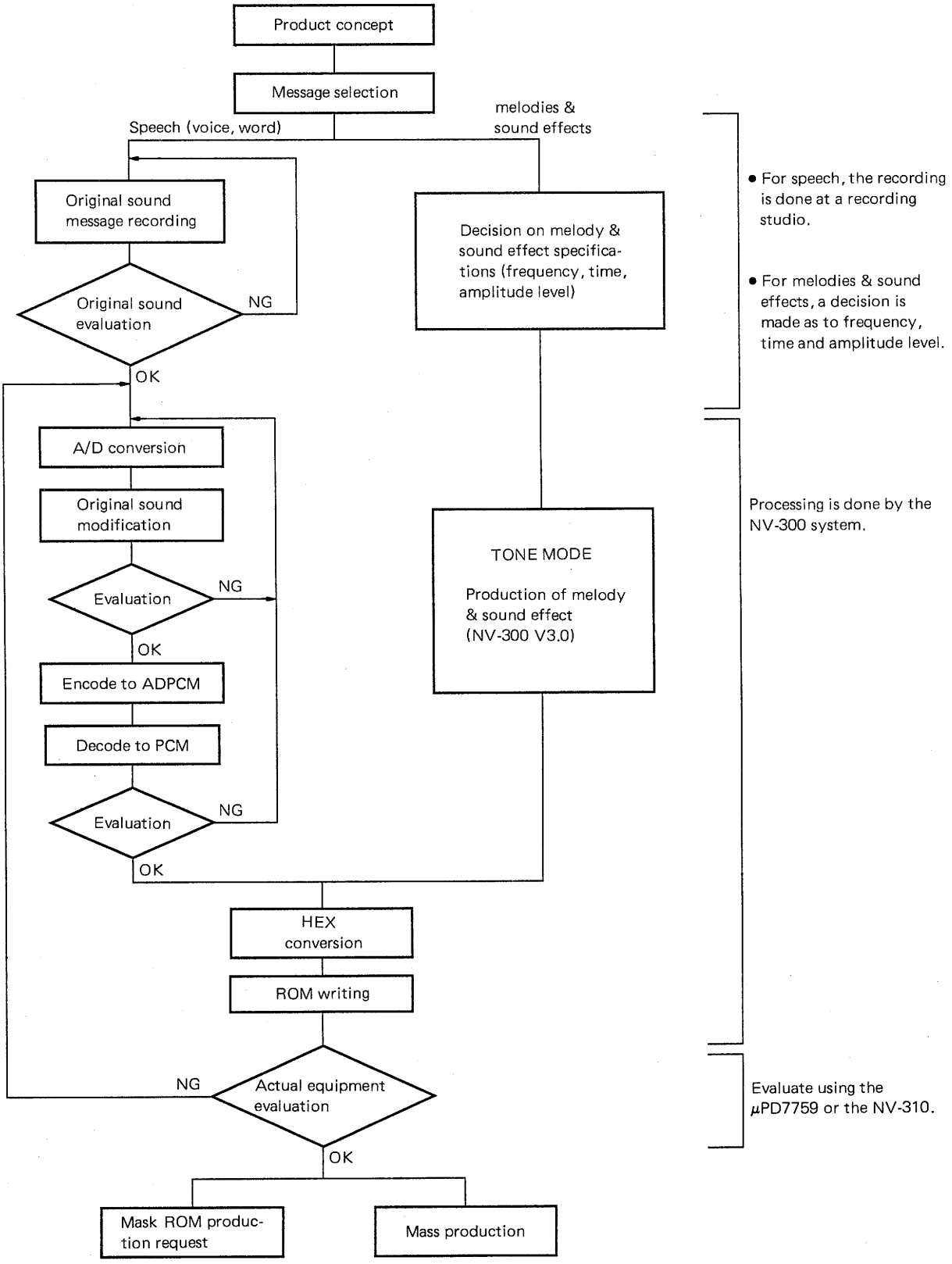
1.4 μPD7755 Family LSI Development Flow

Fig. 1-4 shows the flow of μPD7755 family LSI development. Broadly, the flow is divided into two processes: one that generates speech data from original analog sounds, and one that creates a mask ROM if the LSI is to incorporate one.

The speech data generation process, generally known as speech analysis processing, is implemented at NEC on the basis of the specifications suggested by customers. The customers are also free to execute this process by themselves with the aid of the optional speech analysis tool NV-300.

The commercial production process (including mask ROM making) is exactly the same as that for general microcomputers.

Fig. 1-4 Development flow and allotment



CHAPTER 2 PIN FUNCTIONS

2.1 Pin Configurations

Figs. 2-1 and 2-2 show the pin configurations of the two models of μPD7755, 7756A, 7757, and 7758A each.

Fig. 2-1 μPD7755C, 7756AC, 7757C, and 7758ACR pin configuration (Top view)

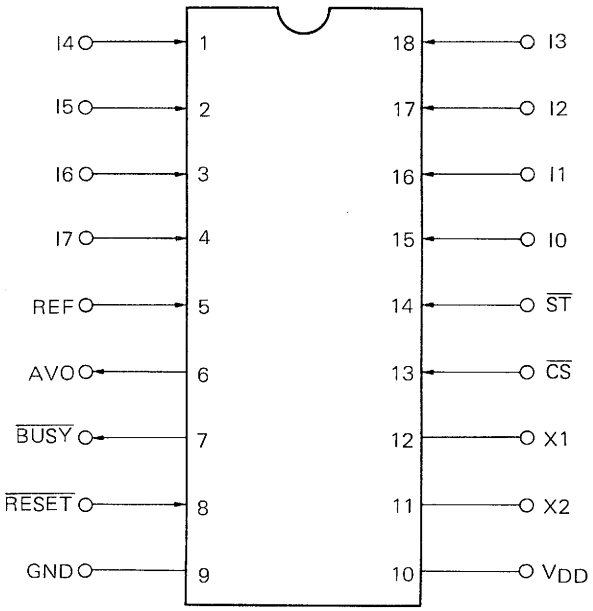
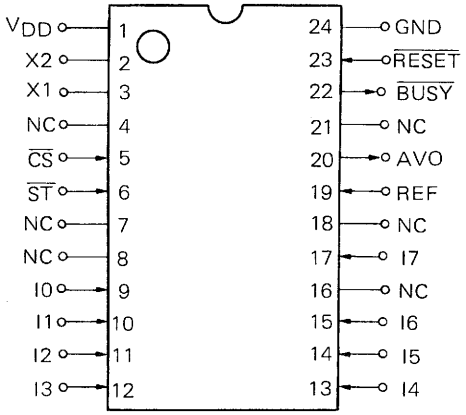


Fig. 2-2 μPD7755G, 7755GT, 7756AG, 7756AGT, 7757G, 7757GT, 7758AG and 7758AGT pin configuration (Top view)



Figs. 2-3 and 2-4 show the pin configurations of the two models of μPD77P56.

Fig. 2-3 μPD77P56CR pin configuration (Top view)

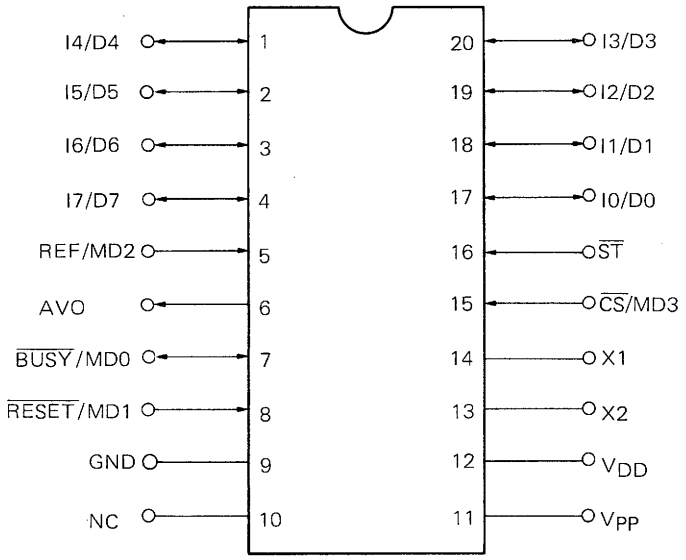
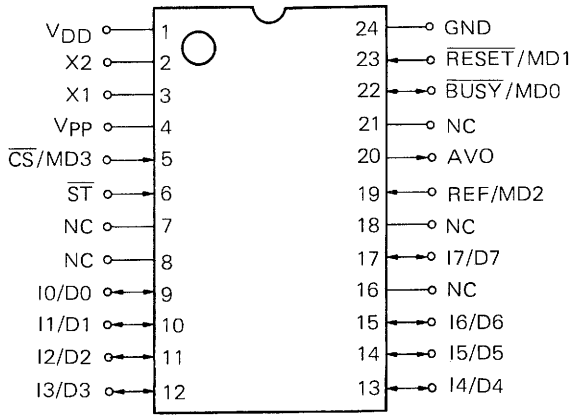


Fig. 2-4 μPD77P56G pin configuration (Top view)



Figs. 2-5 and 2-6 show the pin configurations of the two models of μPD7759.

Fig. 2-5 μPD7759C pin configuration (Top view)

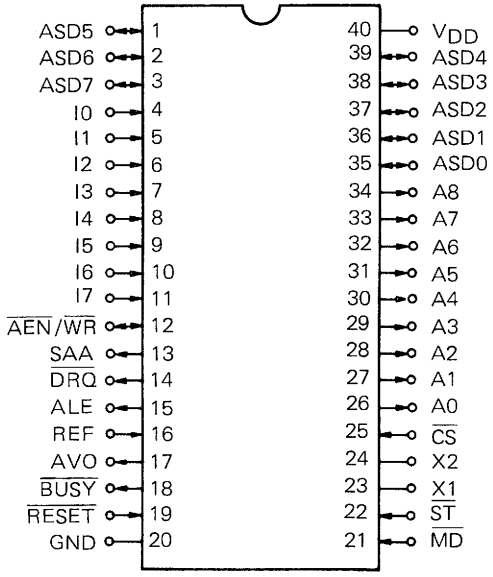
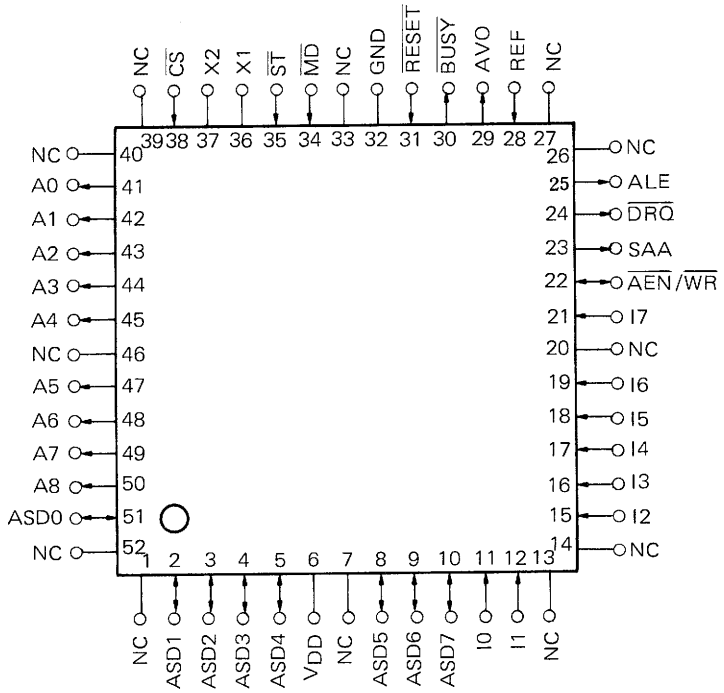


Fig. 2-6 μPD7759GC-3BH pin configuration (Top view)



2.2 μPD7755, 7756A, 7757, and 7758A Pin Functions

Designation	24-pin SOP pin number	18-pin DIP pin number	Input/ Output	Function
V_{DD}	1	10	—	Power supply.
GND	24	9	—	Ground.
X1	3	12	—	Ceramic resonator inputs for clock generation. An external clock may be used. If an external clock is used, X1 is used for clock input and X2 should be left open. X1 is Low-level and X2 is High-level when the LSI is in the standby mode.
★ X2	2	11	—	
$\overline{RESET}$	23	8	Input	Used to reset the LSI. $\overline{RESET}$ must be at low level for 12 clock cycles (oscillation clock). After standby mode is released, $\overline{RESET}$ must be low level more than 12 clocks after clock oscillation becomes stable.
REF	19	5	Input	Used to input the D/A converter reference current. The sink-load current input causes the output current of the D/A converter to change. The D/A converter reference current is passed to V_{DD} via a resistor. In standby mode, REF is set to high impedance.
AVO	20	6	Output	Analog speech signal output. Unipolar open drain type. The output current is reduced to 0 when the LSI is in the standby mode.
$\overline{BUSY}$	22	7	Output	Used to output the low-level active $\overline{BUSY}$ signal. When inputting start signal, it outputs low level signal. $\overline{ST}$ is invalid while $\overline{BUSY}$ is low. In standby mode, $\overline{BUSY}$ is set to high impedance.
$\overline{CS}$	5	13	Input	Used to input a chip select signal. A low on $\overline{CS}$ enables $\overline{ST}$.

Designation	24-pin SOP pin number	18-pin DIP pin number	Input/ Output	Function
$\overline{ST}$	6	14	Input	Used to input a start signal. When $\overline{ST}$ goes low while $\overline{CS}$ is at a low level, the LSI starts synthesizing the message specified by I0 to I7.
I0 I1 I2 I3 I4 I5 I6 I7	9 10 11 12 13 14 15 17	15 16 17 18 1 2 3 4	Input	Used to input the message selection code. The message selection code signals are positive logic. Ground the pins not used. These pins are connected to the internal latch circuit which latches I0 to I7 data at the rising edge of the $\overline{ST}$ input. In standby mode, set the input of these pins to either a high or low level. If these are biased at or near the typical CMOS switch point, causing excess current drain.
NC	Omitted	–	–	No connection.

2.3 μPD77P56 Pin Functions

2.3.1 Pin functions during speech synthesis

Designation	24-pin SOP pin number	20-pin DIP pin number	Input/ Output	Function
V_{DD}	1	12	—	Power supply (2.7 to 5.5 V).
GND	24	9	—	Ground.
X1	3	14	—	Ceramic resonator inputs for clock generation. An external clock may be used. If an external clock is used, X1 is used for clock input and X2 should be left open. X1 is Low-level and X2 is High-level when the LSI is in the standby mode.
★ X2	2	13	—	
$\overline{RESET}$	23	8	Input	Used to reset the LSI. $\overline{RESET}$ must be at low level for 12 clock cycles (oscillation clock). After standby mode is released, $\overline{RESET}$ must be low level more than 12 clocks after clock oscillation becomes stable.
REF	19	5	Input	D/A converter reference current pin. Maximum output current of the D/A converter is approx. 34 times the REF pin input current. The D/A converter reference current is passed to V_{DD} via a resistor. In standby mode, REF is set to high impedance.
AVO	20	6	Output	Analog speech signal output. Unipolar open drain type. The output current is reduced to 0 when the LSI is in the standby mode.
$\overline{BUSY}$	22	7	Output	Used to output the low-level active $\overline{BUSY}$ signal. When synthesizing speech data, it outputs low level signal. $\overline{ST}$ is invalid while $\overline{BUSY}$ is low. In standby mode, $\overline{BUSY}$ is set to high impedance.
$\overline{CS}$	5	15	Input	$\overline{ST}$ becomes valid when $\overline{CS}$ is low level.

Designation	24-pin SOP pin number	20-pin DIP pin number	Input/ Output	Function
$\overline{ST}$	6	16	Input	Used to input a start signal. When $\overline{ST}$ goes low while $\overline{CS}$ is at a low level, the LSI starts synthesizing the message specified by I0 to I7.
I0 I1 I2 I3 I4 I5 I6 I7	9 10 11 12 13 14 15 17	17 18 19 20 1 2 3 4	Input	Used to input the message selection code. The message selection code signals are positive logic. Ground the pins not used. These pins are connected to the internal latch circuit which latches I0 to I7 data at the rising edge of the $\overline{ST}$ input. In standby mode, set the input of these pins to either a high or low level. If these are biased at or near the typical CMOS switch point, causing excess current drain.
V_{PP}	4	11	—	Same potential as V_{DD}.

2.3.2 One-time PROM pin functions

Pin (Abbreviation)	24-pin SOP pin number	20-pin DIP pin number	I/O	Function
V_{DD}	1	12	–	Power supply (6 V)
GND	24	9	–	Ground
X1	3	14	–	Clock input.
MD0 MD1 MD2 MD3	22 23 19 5	7 8 5 15	Input	Operation mode selection pin for program/verify to PROM.
V_{PP}	4	11	–	High voltage application pin for program/verify to PROM (12.5 V).
D0 D1 D2 D3 D4 D5 D6 D7	9 10 11 12 13 14 15 17	17 18 19 20 1 2 3 4	I/O	8-bit data I/O pin for program/verify to PROM.
$\overline{ST}$	6	16	Input	Set at the low level.

Pins other than the above are grounded by pull-down resistance.

Caution AVO, X2 must be opened.

2.4 μPD7759 Pin Functions

2.4.1 μPD7759 mode common pin functions

Designation	52-pin QFP pin number	40-pin DIP pin number	Input/ Output	Function
V_{DD}	6	40	–	Power supply.
GND	32	20	–	Ground.
X1	36	23	–	Ceramic resonator inputs for clock generation. An external clock may be used. If an external clock is used, X1 is used for clock input and X2 should be left open. X1 is Low-level and X2 is High-level when the LSI is in the standby mode.
X2	37	24	–	
$\overline{RESET}$	31	19	Input	Used to reset the LSI. $\overline{RESET}$ must be at low level for 12 clock cycles (oscillation clock). After standby mode is released, $\overline{RESET}$ must be low level more than 12 clocks after clock oscillation becomes stable.
REF	28	16	Input	Used to input the D/A converter reference current. The sink-load current input causes the output current of the D/A converter to change. The D/A converter reference current is passed to V_{DD} via a resistor. In standby mode, REF is set to high impedance.
AVO	29	17	Output	Analog speech signal output. Unipolar open drain type. The output current is reduced to 0 when the LSI is in the standby mode.
$\overline{BUSY}$	30	18	Output	Used to output the low-level active $\overline{BUSY}$ signal. When inputting start signal, it outputs low level signal. $\overline{ST}$, $\overline{MD}$, $\overline{WR}$ is invalid while $\overline{BUSY}$ is low. In standby mode, $\overline{BUSY}$ is set to high impedance.

2.4.2 μPD7759 stand-alone mode pin functions

Designation	52-pin QFP pin number	40-pin DIP pin number	Input/ Output	Function
$\overline{MD}$	34	21	Input	Must be fixed at the low level.
$\overline{CS}$	38	25	Input	Used to input a chip select signal. A low on $\overline{CS}$ enables $\overline{ST}$.
$\overline{ST}$	35	22	Input	Input while $\overline{CS}$ is low starts speech synthesis of the message specified by I0 to I7. When the LSI is in the standby mode, this signal resets the standby mode and starts speech synthesis.
I0 I1 I2 I3 I4 I5 I6 I7	11 12 15 16 17 18 19 21	4 5 6 7 8 9 10 11	Input	Used to input the message selection code. The message selection code signals are positive logic. Ground the pins not used. These pins are connected to the internal latch circuit which latches I0 to I7 data at the rising edge of the $\overline{ST}$ input. In standby mode, set the input of these pins to either a high or low level. If these are biased at or near the typical CMOS switch point, causing excess current drain.
A0 A1 A2 A3 A4 A5 A6 A7 A8	41 42 43 44 45 47 48 49 50	26 27 28 29 30 31 32 33 34	Output	Used to output the lower 9 bits of the external ROM address.
ASD0 ASD1 ASD2 ASD3 ASD4 ASD5 ASD6 ASD7	51 2 3 4 5 8 9 10	35 36 37 38 39 1 2 3	Input/ Output	① Used to output the upper 8 bits of the external ROM address. ② Used to input 8 bits speech synthesis data from the external ROM. These functions are executed, ① first and ② last, on a time-shared basis.

Designation	52-pin QFP pin number	40-pin DIP pin number	Input/ Output	Function
ALE	25	15	Output	Used to determine the timing with which the upper 8 bits of the external ROM address are externally latched. They must be latched at the falling edge of the signal.
$\overline{AEN}/\overline{WR}$	22	12	Output/ Input	$\overline{AEN}$ Output signal indicating that the address signal is enabled. Used to control the latch circuit for the upper 8 bits of the external ROM address.
SAA	23	13	Output	Goes high-level when reading a message start address.
$\overline{DRQ}$	24	14	Output	Speech synthesizing data request.

2.4.3 μPD7759 slave mode pin functions

Designation	52-pin QFP pin number	40-pin DIP pin number	Input/ Output	Function
$\overline{MD}$	34	21	Input	Slave mode designation pin. Mode transitions are not accepted while speech synthesis is in progress.
$\overline{DRQ}$	24	14	Output	Speech synthesis data request.
$\overline{CS}$	38	25	Input	A low on $\overline{CS}$ enables $\overline{WR}$.
$\overline{AEN}/\overline{WR}$	22	12	Output/ Input	$\overline{WR}$ Used to input a write strobe signal for speech synthesis data.
ASD0	51	35	Input	Used to input speech synthesis data from an external source.
ASD1	2	36		
ASD2	3	37		
ASD3	4	38		
ASD4	5	39		
ASD5	8	1		
ASD6	9	2		
ASD7	10	3		
I0	11	4	Input	Disabled; must be fixed high or low.
I1	12	5		
I2	15	6		
I3	16	7		
I4	17	8		
I5	18	9		
I6	19	10		
I7	21	11		
A0	41	26	Output	Disabled; must be left open.
A1	42	27		
A2	43	28		
A3	44	29		
A4	45	30		
A5	47	31		
A6	48	32		
A7	49	33		
A8	50	34		
SAA	23	13	Output	Disabled; must be left open.
ALE	25	15	Output	Disabled; must be left open.
$\overline{ST}$	35	22	Input	Disabled; must be fixed high.

CHAPTER 3 OPERATION OVERVIEW

3.1 Operation Modes and Their Control

3.1.1 Operation modes

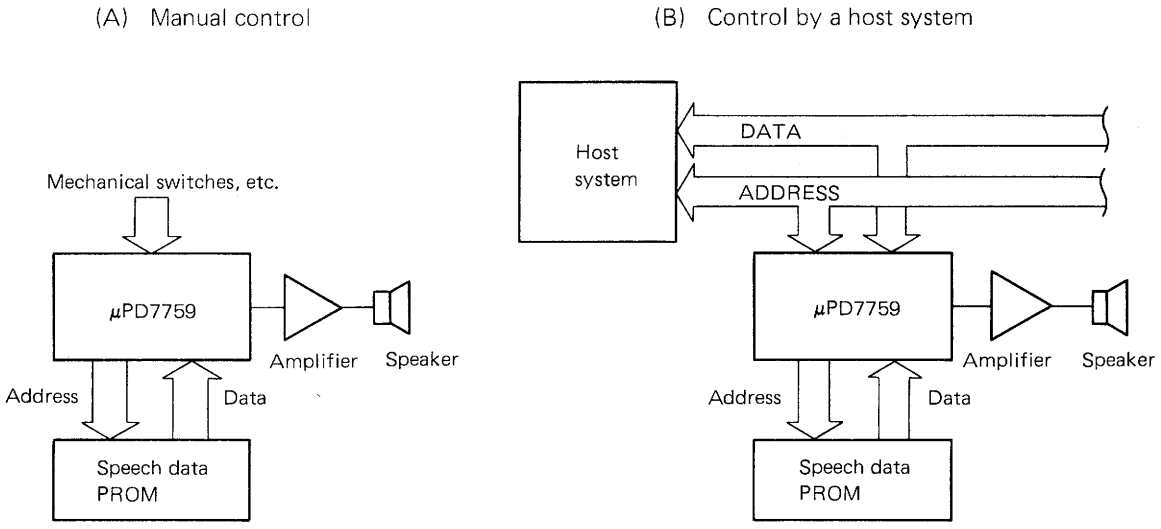
μPD7755 family LSIs support three different modes of operation as follows:

(1) Stand-alone mode

For μPD7755, 7756, 77P56A, 7757, and 7758A with a built-in ROM, the stand-alone mode is the mode in which speech is synthesized.

For μPD7759, which uses an external ROM, speech is synthesized based on the data that is obtained from an external ROM address specified.

Fig. 3-1 Typical system configurations in the stand-alone mode (μPD7759)



(2) Standby mode

In the standby mode, all circuit operations on a speech synthesizer LSI are shut off, except for minimum essential functions, to save the power consumption when the LSI does not synthesize speech for a long time.

In this mode, only the following pin functions are enabled:

(a) $\overline{\text{RESET}}$
(b) $\overline{\text{CS}}$
(c) $\overline{\text{ST}}$
(d) $\overline{\text{WR}}$ (for the μPD7759 only)

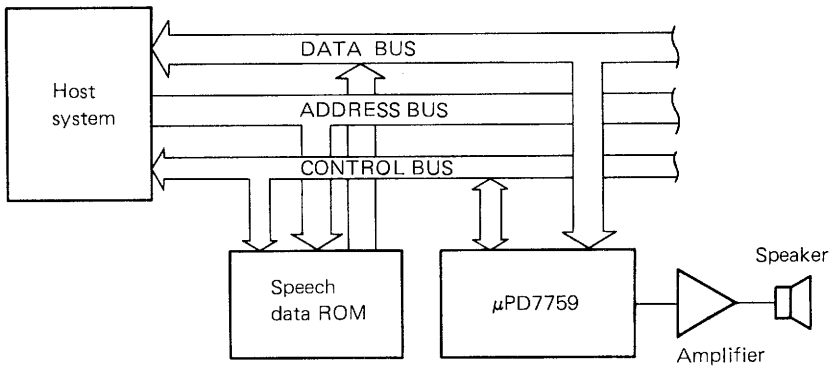
(3) Slave mode (for the μPD7759 only)

In the slave mode, speech is synthesized with a sequential input of speech synthesis data from an external system. The mode permits speech data synthesis over extended periods.

(a) μPD7759 enters the slave mode on detecting the falling edge of an input signal to the $\overline{\text{MD}}$ pin (slave mode setting).
(b) Input signals to the $\overline{\text{MD}}$ pin are ignored while speech synthesis is in progress in the stand-alone mode; that is, the $\overline{\text{BUSY}}$ pin is low.

(c) On entering the slave mode, μPD7759 requests speech data input from the host system with a low on the $\overline{DRQ}$ (data request signal) pin.

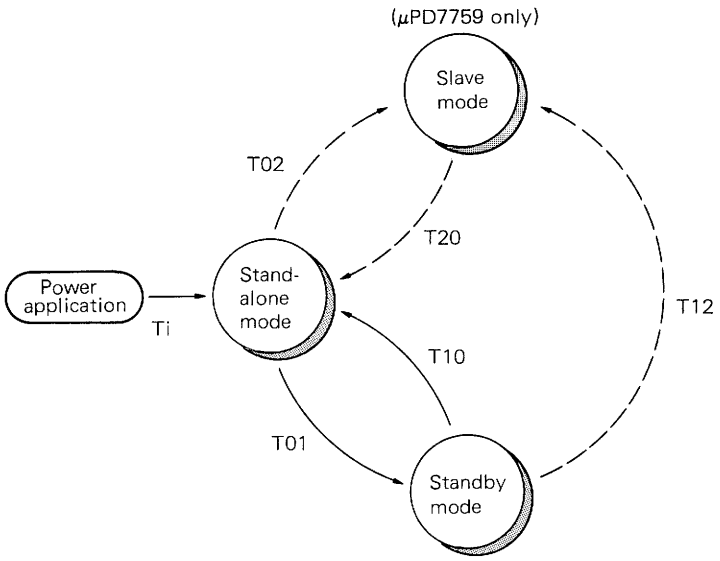
Fig. 3-2 Typical system configuration in the slave mode



3.1.2 Operation mode control

The paths of transition among the three operation modes of the μPD7755 family LSIs, that is, stand-alone mode, standby mode, and slave mode (for μPD7759 only), are shown below.

Fig. 3-3 μPD7755 family LSI state transitions



(1) Transition . . . Ti

Transition flow	Power application → Stand-alone mode
Transition initiated by	$\overline{\text{RESET}}$ pulse input

- The operation mode immediately following power application is unpredictable.
- $\overline{\text{RESET}}$ pulse input brings the LSI into the stand-alone mode.
- The $\overline{\text{RESET}}$ pulse must be latched for at least 12 clocks after clock oscillation at the X1 pin is stabilized.

(2) Transition . . . T01

Transition flow	Stand-alone mode → Standby mode
Transition initiated by	No operation takes place after the end of speech synthesis.

- If no $\overline{\text{RESET}}$, $\overline{\text{CS}}$, or $\overline{\text{ST}}$ signal is input after the end of speech synthesis, the LSI enters the standby mode in about 3 seconds (when operating at a clock frequency of 640 kHz).

(3) Transition . . . T02 (for the μPD7759 only)

Transition flow	Stand-alone mode → Slave mode
Transition initiated by	An input low on the $\overline{\text{MD}}$ pin (mode setting)

- An input low on the $\overline{\text{MD}}$ pin is required for each run of speech synthesis.

(4) Transition . . . T10

Transition flow	Standby mode → Stand-alone mode
Transition initiated by	1. $\overline{\text{RESET}}$ pulse input, or 2. $\overline{\text{ST}}$ (synthesis start) pulse input, in which instance the $\overline{\text{CS}}$ pin must be low

- Since the oscillation circuit is halted while the LSI is in the standby mode, the transition does not take place until clock oscillation is stabilized. The transition takes a maximum of 80 ms (when the LSI is operating at a clock frequency of 640 Hz).

(5) Transition . . . T12

Transition flow	Standby mode → Slave mode
Transition initiated by	An input low on the $\overline{\text{MD}}$ pin (mode setting)

(6) Transition . . . T20

Transition flow	Slave mode → Stand-alone mode
Transition initiated by	1. A transition takes place automatically after the end of speech synthesis, or 2. $\overline{\text{RESET}}$ pulse input

- After the end of speech synthesis, the LSI enters the stand-alone mode, regardless of the level of the $\overline{\text{MD}}$ pin. A high to low transition on the $\overline{\text{MD}}$ pin is required to bring the LSI back into the slave mode.
- $\overline{\text{RESET}}$ pulse input during the execution of speech synthesis forces a mode transition, generating noise in the analog output signals.

3.2 Specifying Synthesized Messages

With an 8-bit bus, 10 to 17, μPD7755 family LSIs permit up to 256 kinds of messages to be externally specified for synthesis in the stand-alone mode.

The data input through 10 to 17 is called "message select code".

The message select code requested by the user is allocated to the corresponding message when the speech data ROM is produced.

Note: – If no corresponding data has been allocated for the message select code generated during synthesizing operation in advance, no audio signal is output.

– Two or more message select codes can be allocated for one message.

Figs. 3-4 and 3-5 are timing charts for specifying synthesized messages. In Fig. 3-4, control is exercised by the use of the $\overline{CS}$ and $\overline{ST}$ pins. In Fig. 3-5, control is exercised by the use of the $\overline{ST}$ pin only, with the $\overline{CS}$ pin fixed at the low level.

Fig. 3-4 Message specification timing chart (1)

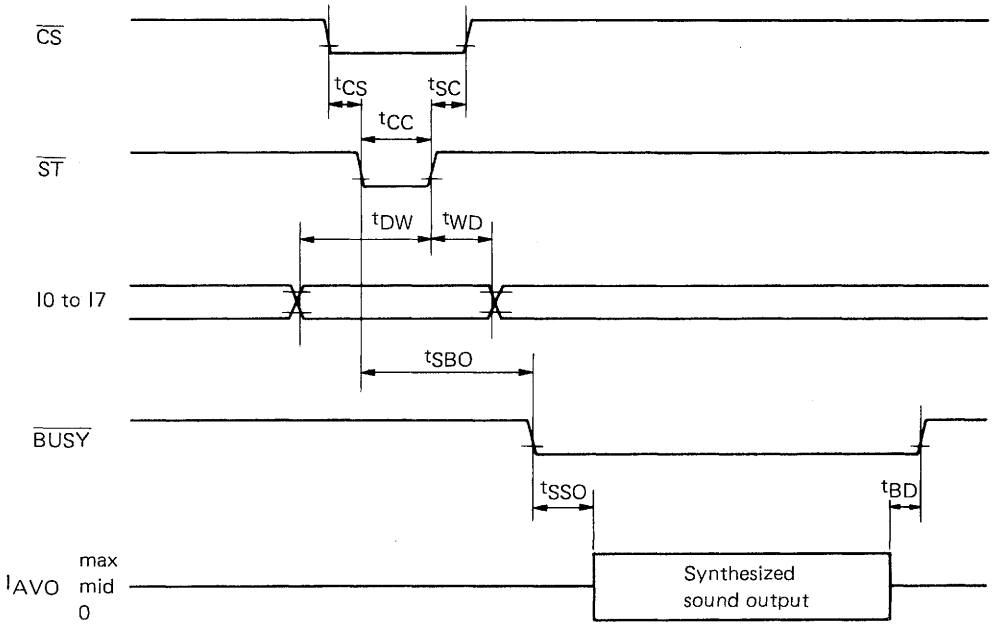
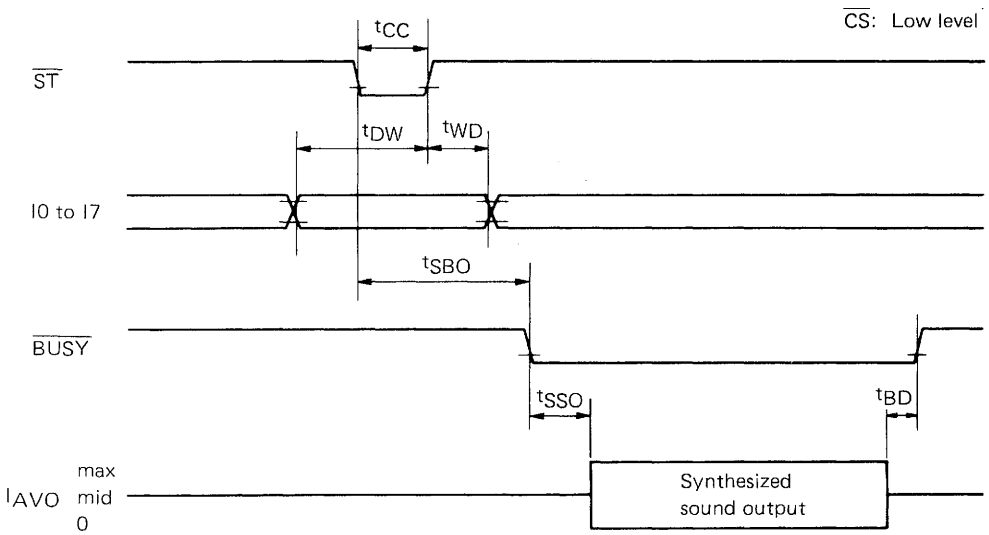


Fig. 3-5 Message specification timing chart (2)



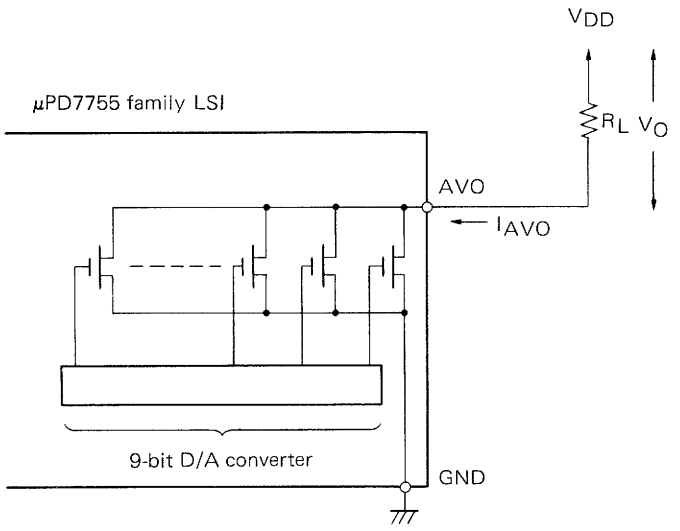
3.3 Analog Output Circuit Operations

The analog output circuits of the three μPD7755 family LSIs are constructed in the same way. The following describes the construction of the μPD7755 family LSI's analog output section and its adjustment procedure.

3.3.1 D/A converter configuration

The D/A converter built in each μPD7755 family LSI is of the unipolar current output type, with a 9-bit resolution. Since the analog output pin (AVO pin), or the D/A converter output, has an open drain structure, voltage output can be obtained by connecting an external resistor (R_L) to the D/A converter. (See Fig. 3-6.)

Fig. 3-6 μPD7755 family LSI analog output circuit configuration



During speech analysis, the output current vascillates at around one half of the full-scale output current of the built-in D/A converter; that is, the output current during silent periods equals one half of the full-scale output current.

3.3.2 Adjusting the output current of the D/A converter

The output current of the D/A converter can be adjusted with the voltage applied to the REF pin. In practice, this is effected by inserting a resistor between V_{DD} and the REF pin as shown in Fig. 3-7.

Figs. 3-8 and 3-9 show the relationship of the voltage on the REF pin (V_{REF}) with the reference input current (I_{REF}) and the D/A converter output current (I_{AVO}).

When the amplifier connected to the AVO pin has a high input impedance (several kΩ or higher), the value of R_{REF} can be determined with reference to Fig. 3-8.

On the basis of this figure, I_{REF} ranges from 60 to 80 μA (its intersection with the R_{REF} = 50 kΩ load line) if a 50 kΩ resistor is used as R_{REF} when V_{DD} = 5 V. On the other hand, since the maximum value of I_{AVO} is 32 to 36 times higher than I_{REF}, it follows that I_{AVO} ranges from 1.9 to 2.9 mA.

Since the synthesized sound output level varies by about 4 dB in this instance, a fixed resistor can be used as R_{REF} if proper attention is given to its resistance accuracy, unless uniformity in the synthesized sound output level among different products is required.

When the amplifier connected to the AVO pin has a low input impedance, the value of R_{REF} can be determined with reference to Fig. 3-9.

On the basis of this figure, I_{AVO} ranges from 12 to 30 mA if a 1 kΩ resistor is used as R_{REF} when V_{DD} = 5 V.

Since variations in the synthesized sound output level amount to about 8 dB, use of a variable resistor as R_{REF} to adjust the output level is recommended.

Fig. 3-7 D/A converter reference current

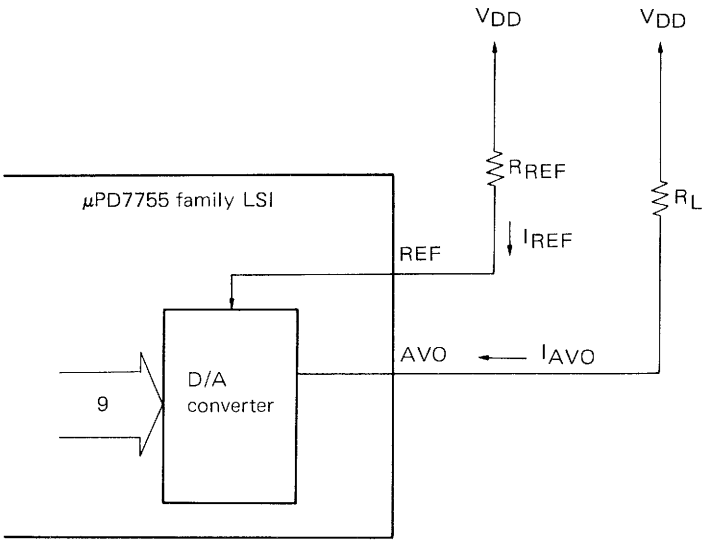


Fig. 3-8 V_{REF} vs. I_{REF} and I_{AVO}

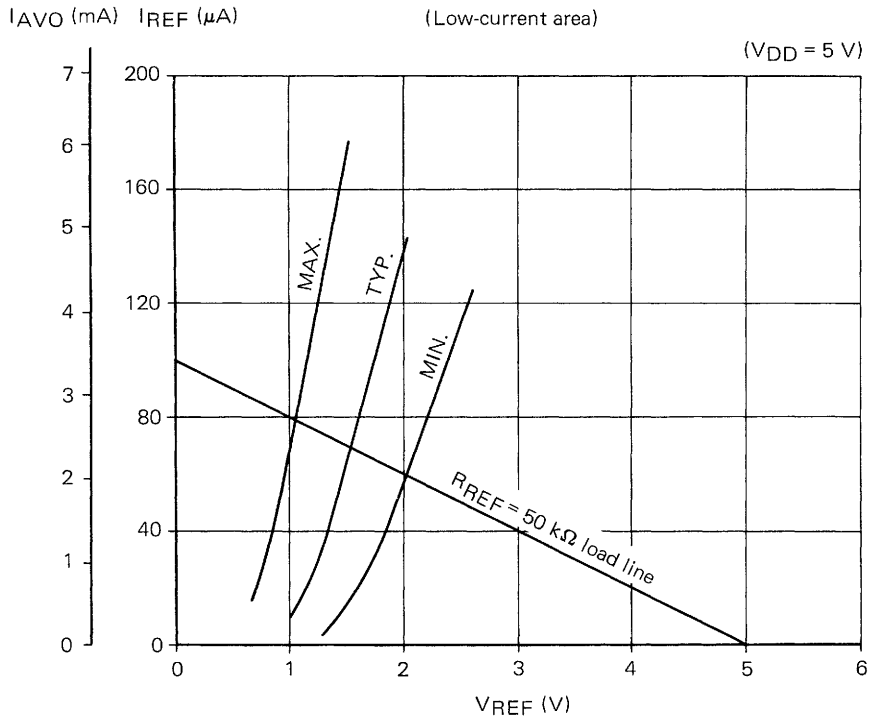
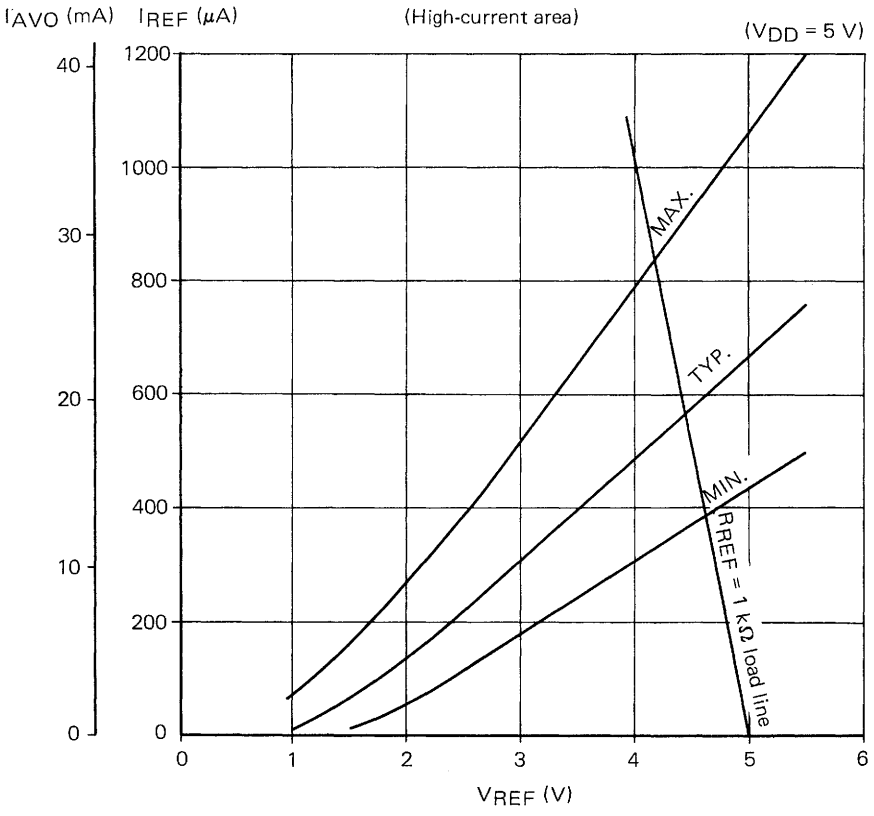


Fig. 3-9 V_{REF} vs. I_{REF} and I_{AVO}



Since the output current (I_{AVO}) of the AVO pin is a drain current, a load resistor (R_L) is connected to V_{DD}.

In this case, it is necessary to set the voltage of AVO shown in Fig. 3-6 within the range in which the output transistor in the D/A converter operates as a constant-current source.

This range will be:

V_{DD} = 5 V: 1.5 V to V_{DD}

V_{DD} = 3 V: 1 V to V_{DD}

Set the load resistance and the output current to keep the value of AVO within this range.

If the output current (I_{AVO}) needs adjustment, follow the procedures below.

(1) Specify message synthesis (to output the middle-point current to the D/A converter).
(2) Supply a reset signal within 3 seconds after the end of synthesized sound output (to prevent the LSI from entering the standby mode).
(3) Adjust R_{REF} for the specified AVO voltage.

3.3.3 D/A converter in the standby mode

Since μPD7755 family LSIs use a unipolar 9-bit D/A converter, they carry half the full-scale output current flow during operation even in the absence of signals.

In the standby mode, the input of the D/A converter is reduced to 0 so the output current equals 0.

To prevent pop noises caused by abrupt changes in the D/A converter output current during operation to standby mode transitions, the output current is gradually reduced immediately before the LSI enters the standby mode. (See Fig. 3-10.)

During standby mode to operation mode transitions, clock oscillation is started by a standby reset signal generated by the $\overline{CS}$ and $\overline{ST}$ inputs. After clock oscillation is stabilized, the output current is gradually increased to half of the full-scale current. (See Fig. 3-11.)

Fig. 3-10 D/A converter output current during transitions to the standby mode

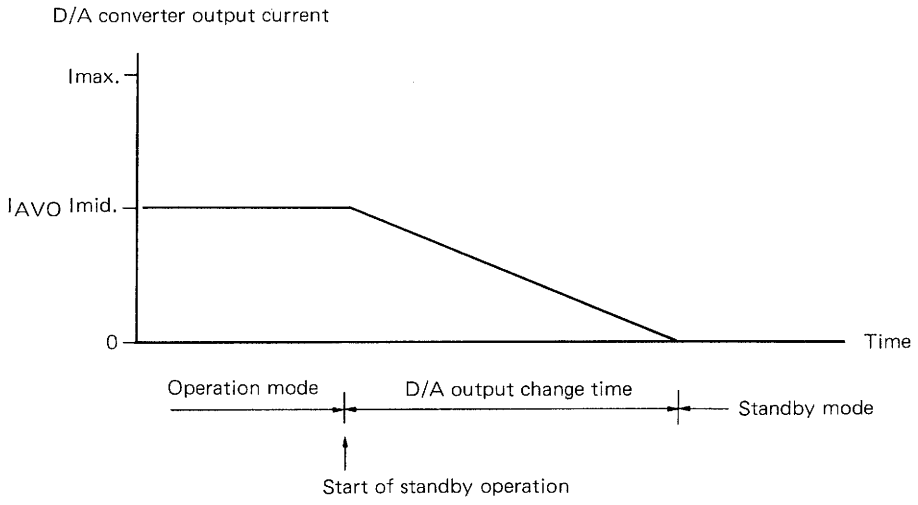
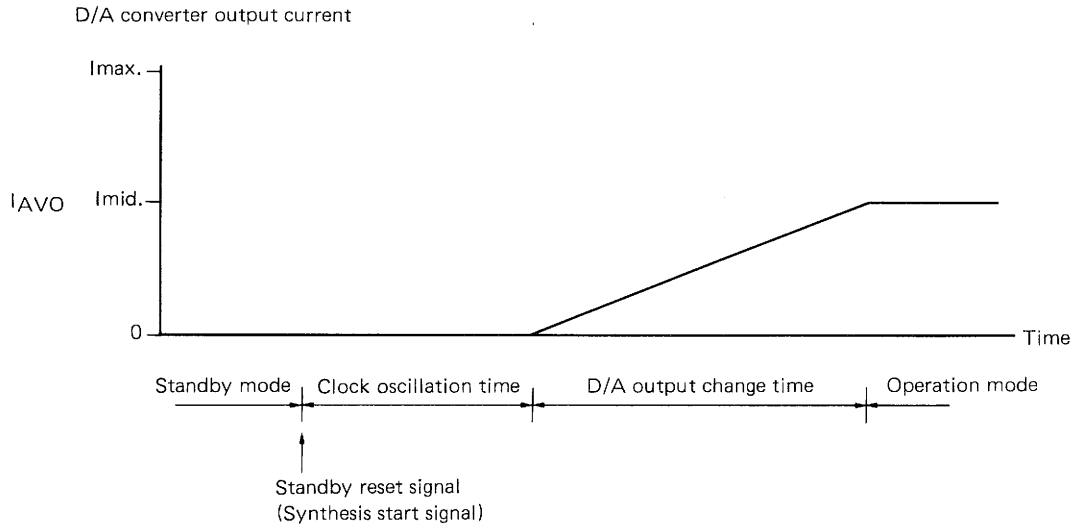


Fig. 3-11 D/A converter output current when the standby mode is reset

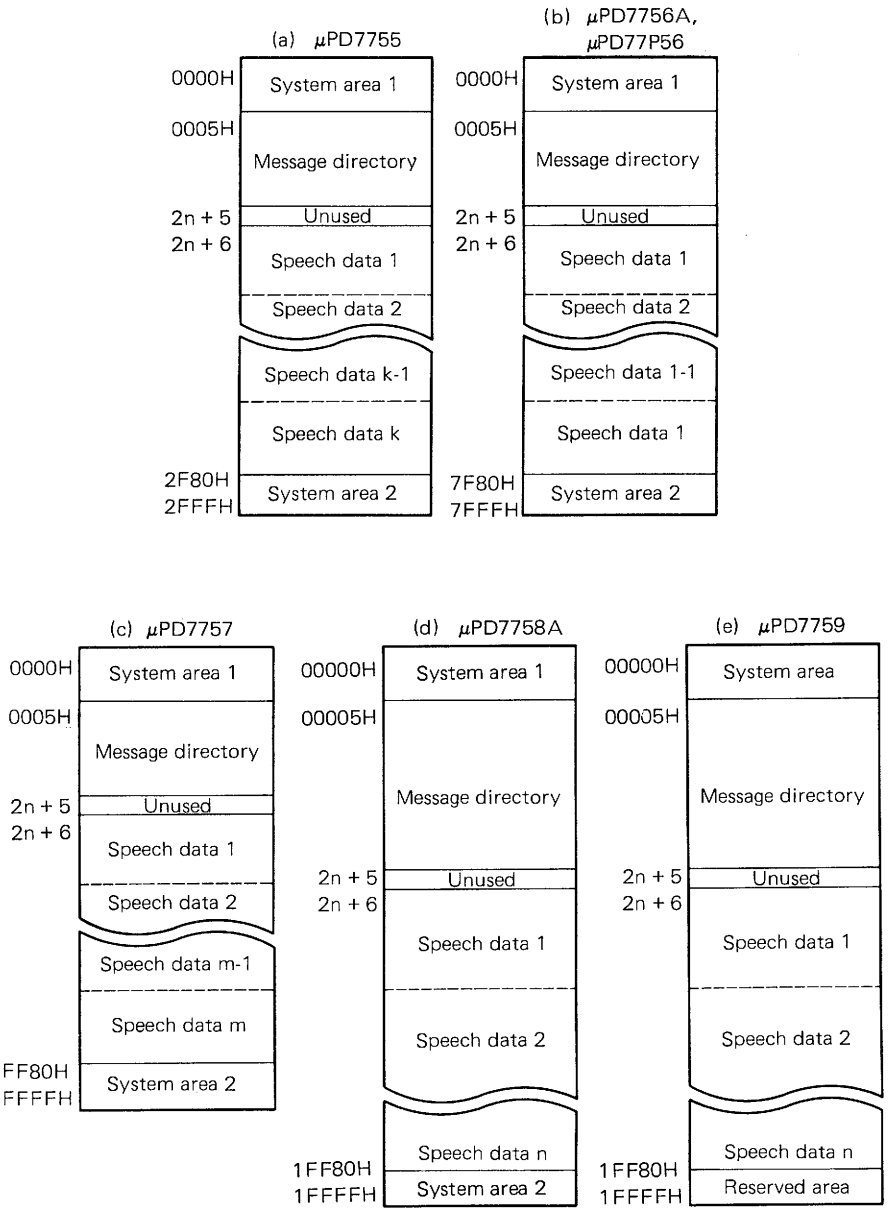


3.4 μPD7759 External Data Interface

3.4.1 μPD7755 family LSI memory map

The internal ROMs in μPD7755, 7756A, 77P56, 7757, and 7758A and the ROM external to μPD7759 in its stand-alone mode are mapped as shown in Fig. 3-12. Since these LSIs, though compatible in speech data, vary in their memory map, data developed for one LSI cannot be directly used for other LSIs.

Fig. 3-12 μPD7755 family LSI memory maps



(1) System area

Constant data used for an LSI is stored in this area.

(2) Reserved area

This area is not available for use, and data is not stored in it.

(3) Speech data area

Coded speech data is stored in this area.

- If the total number of messages involved is n, initial speech data is stored starting at address 2n + 6.
- Data associated with a message is stored starting at an even-numbered address, with the starting data being 00H, 40H, or 80H and the ending data being 00H.

(4) Message directory

The message directory indicates the starting address of the speech data associated with each message.

- The starting address is expressed in 2 bytes, which are stored upper byte first and lower byte last.
- If the message select code assigned to a particular message is J, the starting address of the speech data associated with that message is stored split into address 2J + 5 and address 2J + 6 (for μPD7755, 7756A, 77P56, 7757, and 7758A).

  μPD7759 requires 17 bits to address its external ROM, though its starting address consists only of an even-numbered address, and half the address is stored at the above-mentioned addresses.

3.4.2 μPD7759 slave mode interface

Speech data must be sequentially input from μPD7759 when it is in the slave mode. The input data format is shown in Fig. 3-13. As shown, 4-byte auxiliary data must precede the speech data at the start of synthesis and 3-byte dummy data must follow the speech data at the end of synthesis.

As speech data, the data as described in 3.4.1 can be used as it is.

Fig. 3-13 Slave mode input data

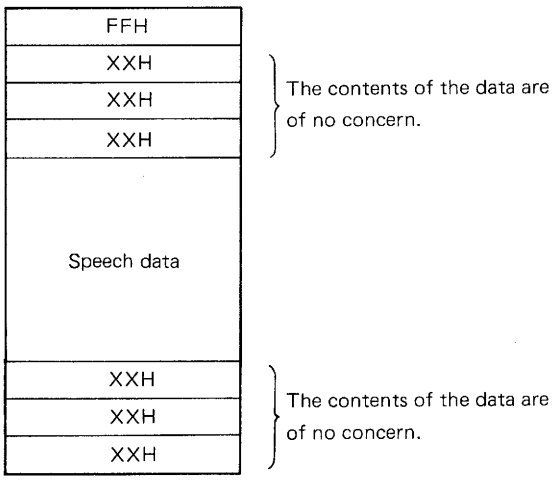


Fig. 3-14 is a timing chart in which one message is synthesized in the slave mode. Fig. 3-15 is a timing chart in which 1-byte speech data is input.

Fig. 3-14 Slave mode timing chart

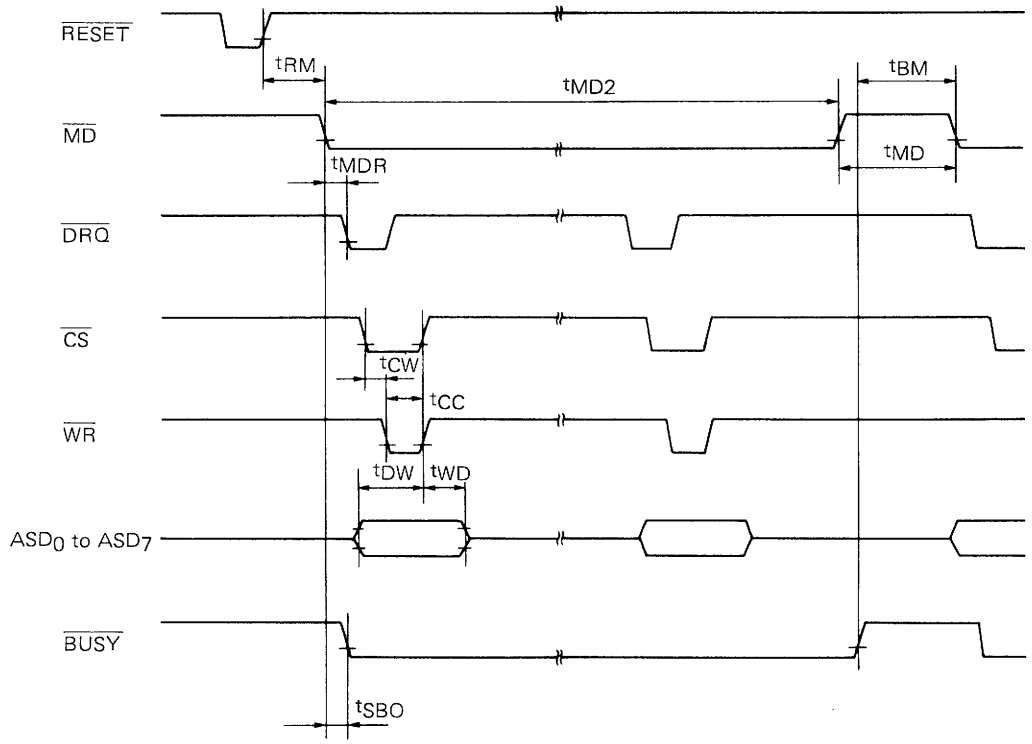
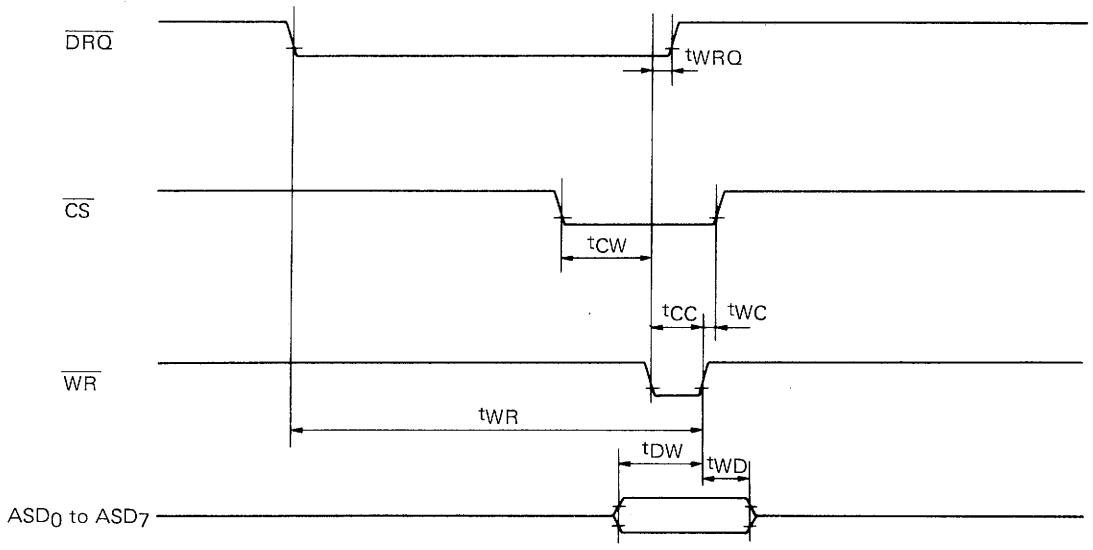


Fig. 3-15 Slave mode data input timing chart



In the μPD7755 family LSIs, each byte of speech data consists of two sets of coded data. As a result, $\overline{\text{DRQ}}$ (data request signal) output from μPD7759 in the slave mode is output at half the sampling frequency interval on the average, exerting an increased burden on the host system. This fact should deserve special attention when hardware configurations in which the system CPU undertakes this operation are used.

★ 3.5 Clock Generator

The clock generator generates clock signals for use within a chip. Connect an external ceramic resonator and capacitors as shown in Fig. 3-16.

An external clock can be used. If an external clock is used, X1 is used for clock input and X2 should be left open. When a μPD7755 family LSI is in standby mode, X1 outputs low level. Therefore, a capacitor which is about 100 pF must be connected in series to X1 as shown in Fig. 3-17 to avoid input of direct current.

In the standby mode, X1 and X2 are fixed low and high, respectively.

Fig. 3-16 Connection of ceramic resonator

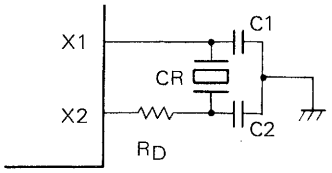


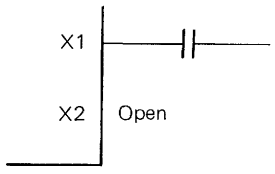
Table 3-1 The value of parameter for each ceramic resonator[Note]

Part number	Manufacturer	C_1 [PF]	C_2 [PF]	R_D [kΩ]
CSB640P	Murata Co., Ltd.	220	220	0
KBR640B	Kyocera Co., Ltd.	220	220	0
CRK640	Toko Co., Ltd.	33	150	9.1
FCR640K2	TDK Co., Ltd.	390	390	0

Note These parameters are for reference only and are not intended for use in actual design-in's. Furthermore, actual parameters may be different from these parameters according to which ceramic resonator is connected with which of μPD7755 family LSIs.

Please inquire the specific data for design-in's from the ceramic resonator manufacturer.

Fig. 3-17 Input of external clock



3.6 Programming and Verifying One-Time PROM

μPD77P56 include a 256K bit one-time PROM as speech data memory. Procedures for programming data to the PROM and verifying the data are described below.

Normal programming and verification can be executed by replacing the socket adapter using the PG-1500 PROM programmer.

3.6.1 PROM operation modes

Applying +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin brings the μPD77P56 into the operation mode that is designated by the MD0 to MD1 pins as described in the table below. The $\overline{ST}$ pin is fixed low.

Table 3-2 PROM operation modes

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
12.5 V	6 V	H	L	H	L	① Program address zero-clear mode
		L	H	H	H	② Program mode
		L	L	H	H	③ Verify mode
		H	X	H	H	④ Program inhibit mode

X: Low or high

Operation mode descriptions

① Program address zero-clear mode

The PROM address is cleared to 0. Note that the address will be reset to 0 if this mode is set even momentarily during mode transitions.

② Program mode

Speech analysis data can be programmed to the PROM. Data is input to D0 – D7.

③ Verify mode

The speech analysis data programmed to the PROM can be verified as it is output from D0 – D7.

④ Program inhibit mode

No operation occurs. When the LSI is switched from one mode to another, this mode may intervene to bypass the program address zero-clear mode.

Note: Constant data used for this LSI is stored in the system area of the memory, from 0001H to 0004H. The data are 5A, A5, 69, and 55.
Then please check the blank of the memory just from 0005H to the end address and program it from 0000H to the end address.

3.6.2 Initialization

To prevent μPD77P56 from entering the write mode the moment V_{DD} and V_{PP} are set to 6 V and 12.5 V. respectively, the program address zero-clear mode setting (Note) is assigned before μPD77P56 enters the PROM operation mode.

Note

MD0	MD1	MD2	MD3
H	L	H	L

3.6.3 Data program timing

PROM program procedure of normal and high speed program is as follows:

Normal program

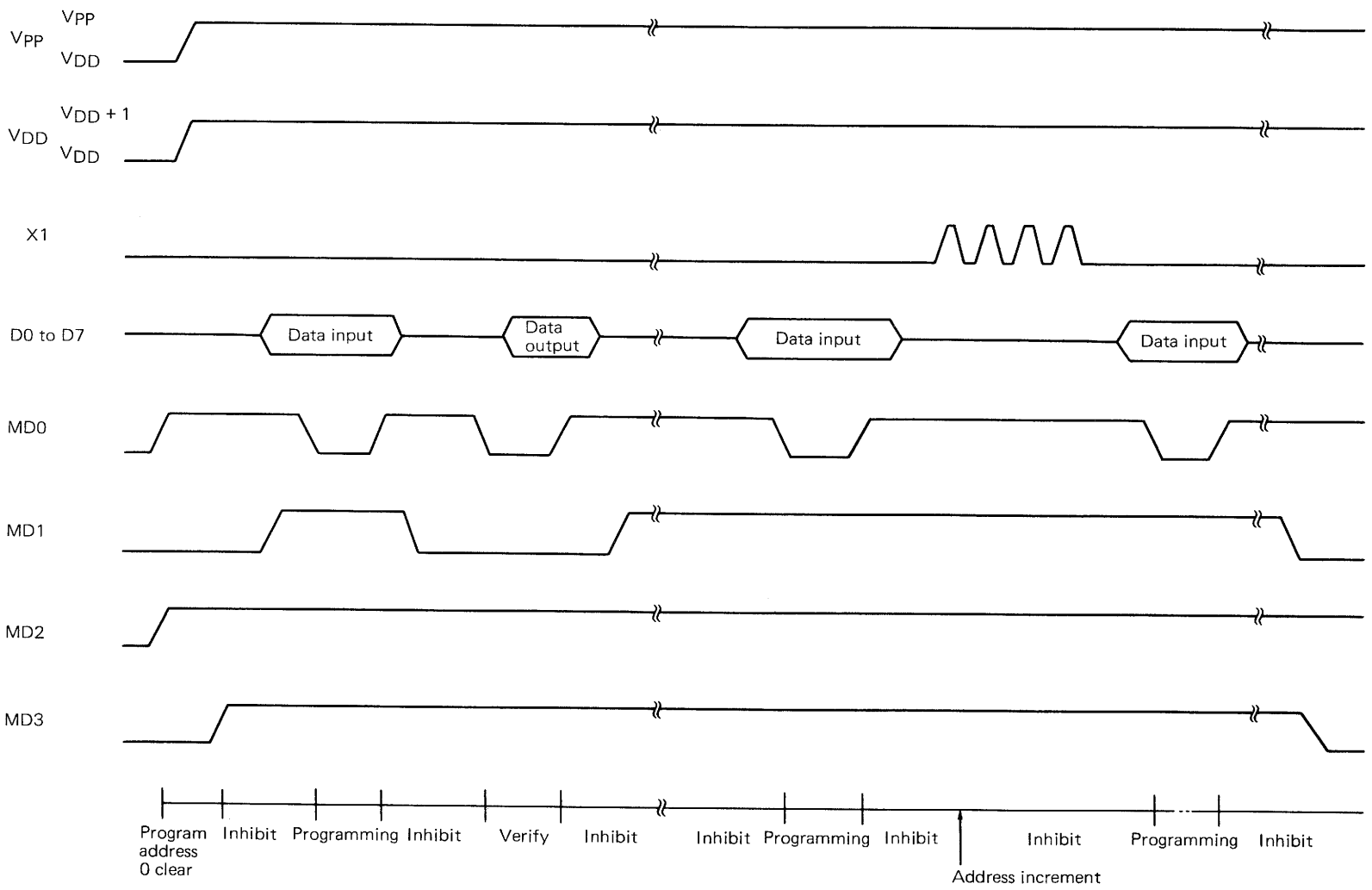
(1) Set $\overline{ST}$ to low level, AVO, X2 pin to OPEN, and X1 pin to low level.
(2) Apply 5 V to V_{DD} and V_{PP}.
(3) 10 μs waiting.
(4) PROM address 0 clear mode.
(5) Apply 6 V and 12.5 V to V_{DD} and V_{PP} respectively.
(6) Program inhibit mode.
(7) Program data in 1 ms of program mode.
(8) Program inhibit mode.
(9) Verify mode: If data has been programmed, go to item (10), if data has not been programmed, repeat items (7) to (9).
(10) Additional programming: X* x 1 ms

* The number of times programmed in item (7) to (9).

(11) Program inhibit mode.
(12) Increment an address by inputting pulse to X1 pin four time.
(13) Repeat (7) to (9) up to the final address.
(14) PROM address 0 clear mode.
(15) Change voltages V_{DD} and V_{PP} to 5 V.
(16) Power off.

Note: Avoid setting the PROM address 0 clear mode when moving to another mode. Figure on the next page shows procedures (2) to (12).

Normal data programming timing



3.6.4 Data readout timing

μPD77P56 can readout data from the PROM in the following sequence:

(1) Set a low on $\overline{ST}$, leave AVO, X2 open, and set a low on the X1 pin.
(2) Supply 5 V to V_{DD} and V_{PP}
(3) Wait for 10 μs.
(4) PROM address 0-clear mode.
(5) Apply 6 V and 12.5 V to V_{DD} and V_{PP}, respectively.
(6) Program inhibit mode.
(7) Verify mode. Output data sequentially at the frequency of clock pulse input to the X1 pin.
(8) Program inhibit mode.
(9) PROM address 0-clear mode.
(10) Change the voltage for V_{DD} and V_{PP} to 5 V.
(11) Power off.

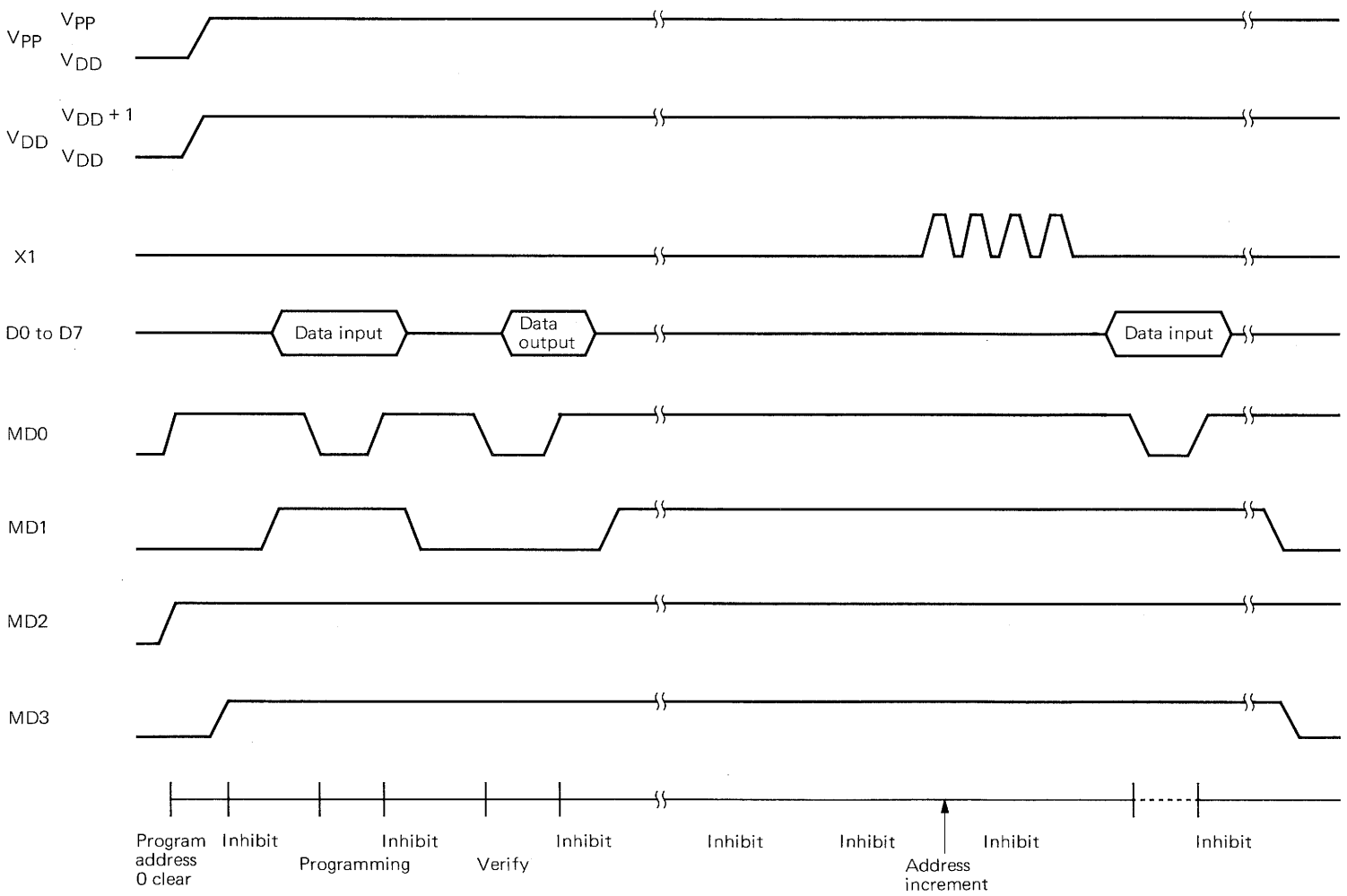
Note: Avoid setting the PROM address 0 clear mode when moving to another mode.
Figure on the 39 page shows procedures (2) to (9).

3.6.5 High speed program

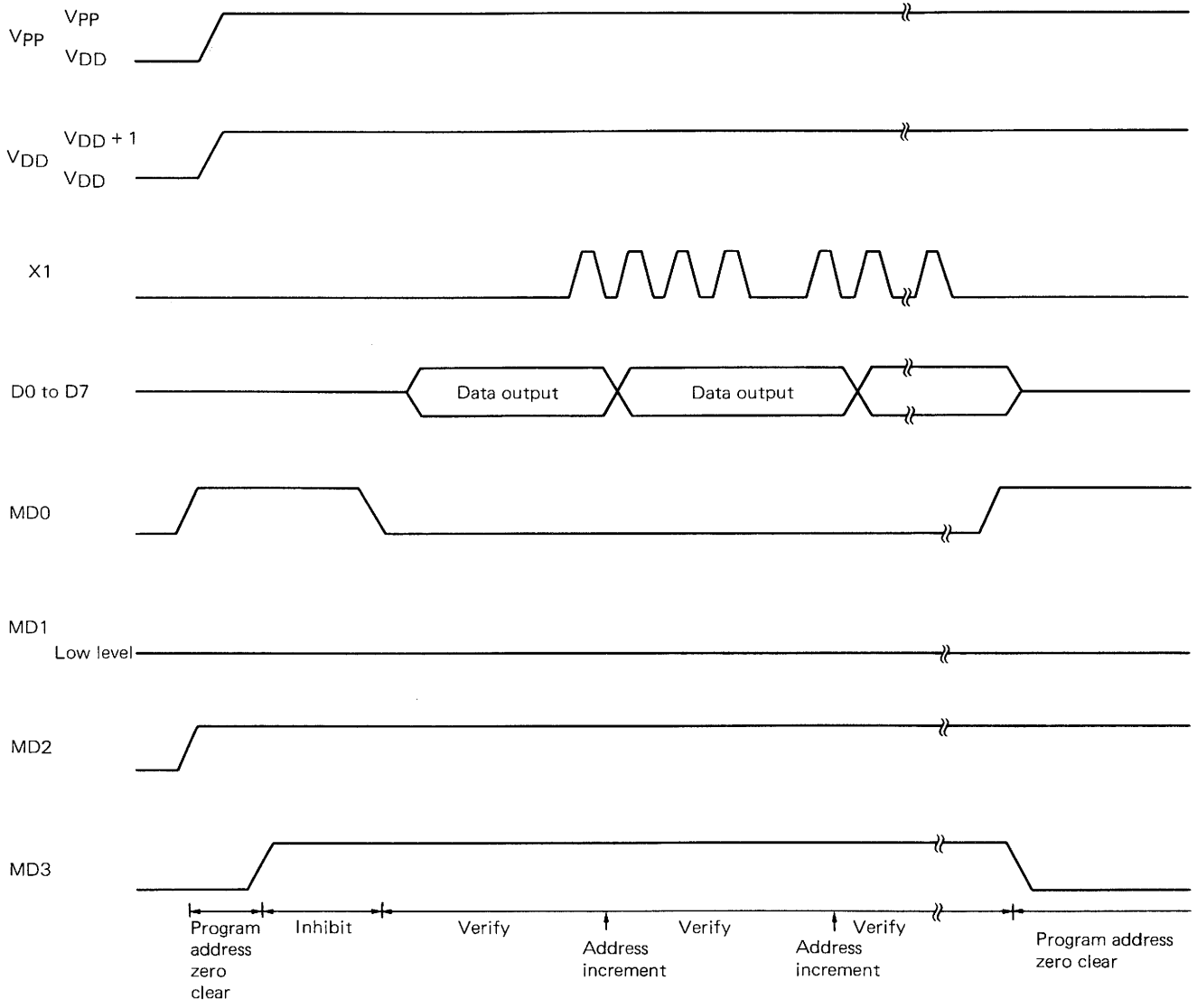
(1) Set $\overline{ST}$ to low level, AVO, X2 pin to OPEN, and X1 pin to low level.
(2) Apply 5 V to V_{DD} and V_{PP}.
(3) 10 μs waiting.
(4) PROM address 0 clear mode.
(5) Apply 6 V and 12.5 V to V_{DD} and V_{PP} respectively.
(6) Program inhibit mode.
(7) Program data in 250 μs of program mode.
(8) Program inhibit mode.
(9) Verify mode: If data has been programmed, go to item (10), if data has not been programmed, repeat items (7) to (9).
(10) Program inhibit mode.
(11) Increment an address by inputting pulse to X1 pin four time.
(12) Repeat (7) to (11) up to the final address.
(13) PROM address 0 clear mode.
(14) Change voltages V_{DD} and V_{PP} to 5 V.
(15) Power off.

Note: Avoid setting the PROM address 0 clear mode when moving to another mode. Figure on the next page shows procedures (2) to (11).
This high speed program is different from the usual high speed program of UVPROM's.

High speed data programming timing



Data readout timing



CHAPTER 4 APPLICATION CIRCUIT EXAMPLES

This chapter describes examples of typical application circuits that embody μPD7755 family LSIs.

Please note that these example circuits are not intended for commercial production that allows for component deviations and temperature characteristics. NEC assumes no responsibility for the use of patents on the circuits shown.

4.1 Control Circuits

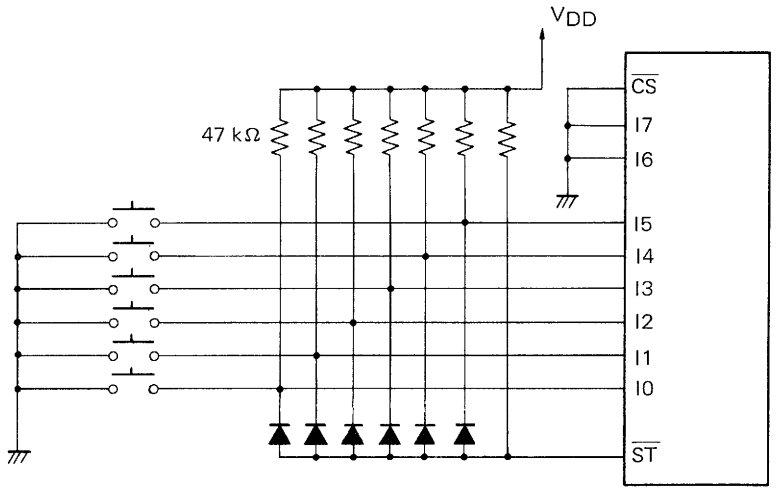
4.1.1 Simplified message select circuit

Fig. 4-1 shows a simplified message select circuit with manual switches that connects to a μPD7755 family LSI.

Switches having long make times are suitable.

Since the μPD7755 family LSIs have eight message select lines each, message select codes can be assigned as 2^n (n = 0, 1, ... 7) to have a one-to-one correspondence between the select lines and messages. Priority may also be assigned to the messages by the message select codes.

Fig. 4-1 Simplified messages select circuit example



μPD7755 family LSI
(stand-alone mode)

4.1.2 Control by microcomputer

Fig. 4-2 shows a typical control circuit organized in a 4-bit single-chip microcomputer of 75X series. In this example, the μPD7755 family LSI is controlled by using the 75X series ports P00, P40 to P43, and P50 to P53. Fig. 4-3 shows the control procedure executed from the 75X series.

Fig. 4-2 Typical control circuit organized in the 75X series

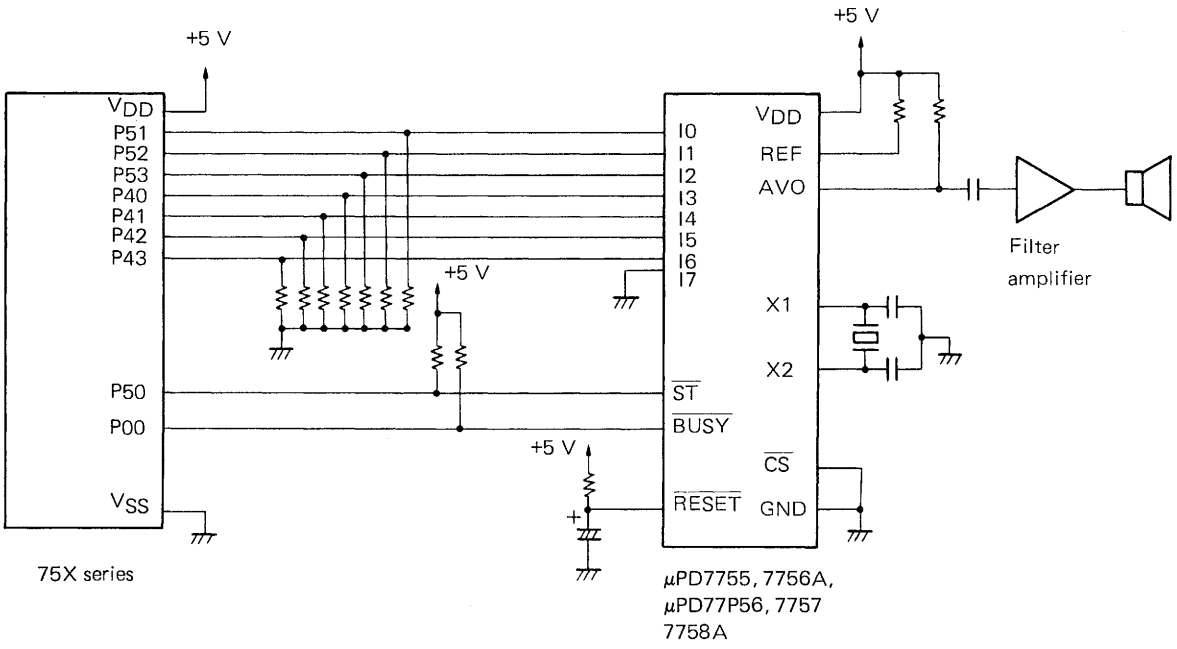


Fig. 4-3 Control procedure in the 75X series

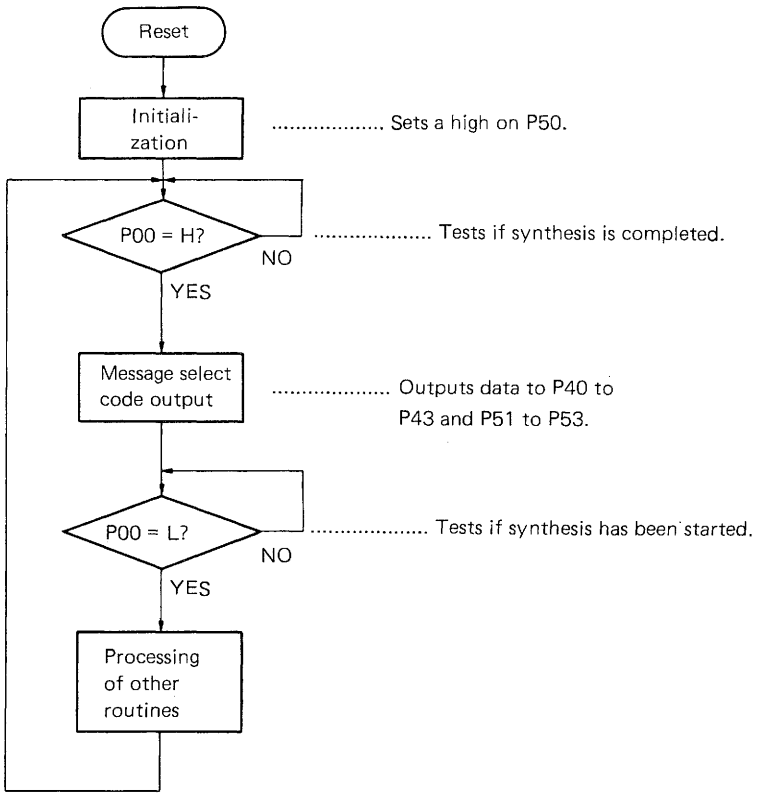
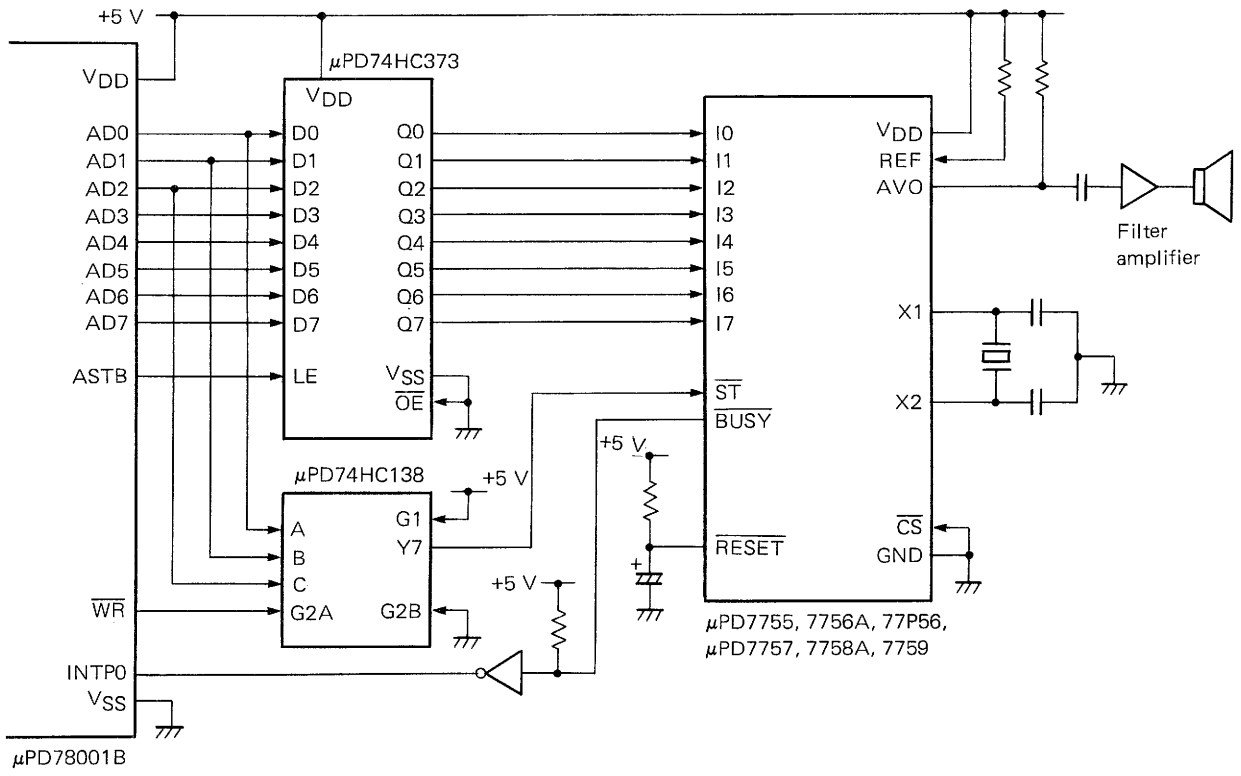


Fig. 4-4 shows a typical circuit that connects to a system based on an 8-bit single-chip microcomputer μPD78001B. In this example, the speech synthesizer LSI is allocated to μPD78001B I/O address "xxxx xxxx xxxx x000." The control procedure is the same as that for the 75X series, except that interrupt is used to detect $\overline{BUSY}$.

Fig. 4-4 Typical control circuit organized in the μPD78001B ★



Caution 1. The $\overline{ST}$ pulse must be at least 350 ns wide.

2. Pullup or pulldown resistors for address/data bus are omitted in this figure. Actually, pullup or pulldown resistors are required between AD0-AD7 of μPD78001B and D0-D7 of μPD74HC373, between Q0-Q7 of μPD74HC373 and I0-I7 of μPD7755 family LSI.

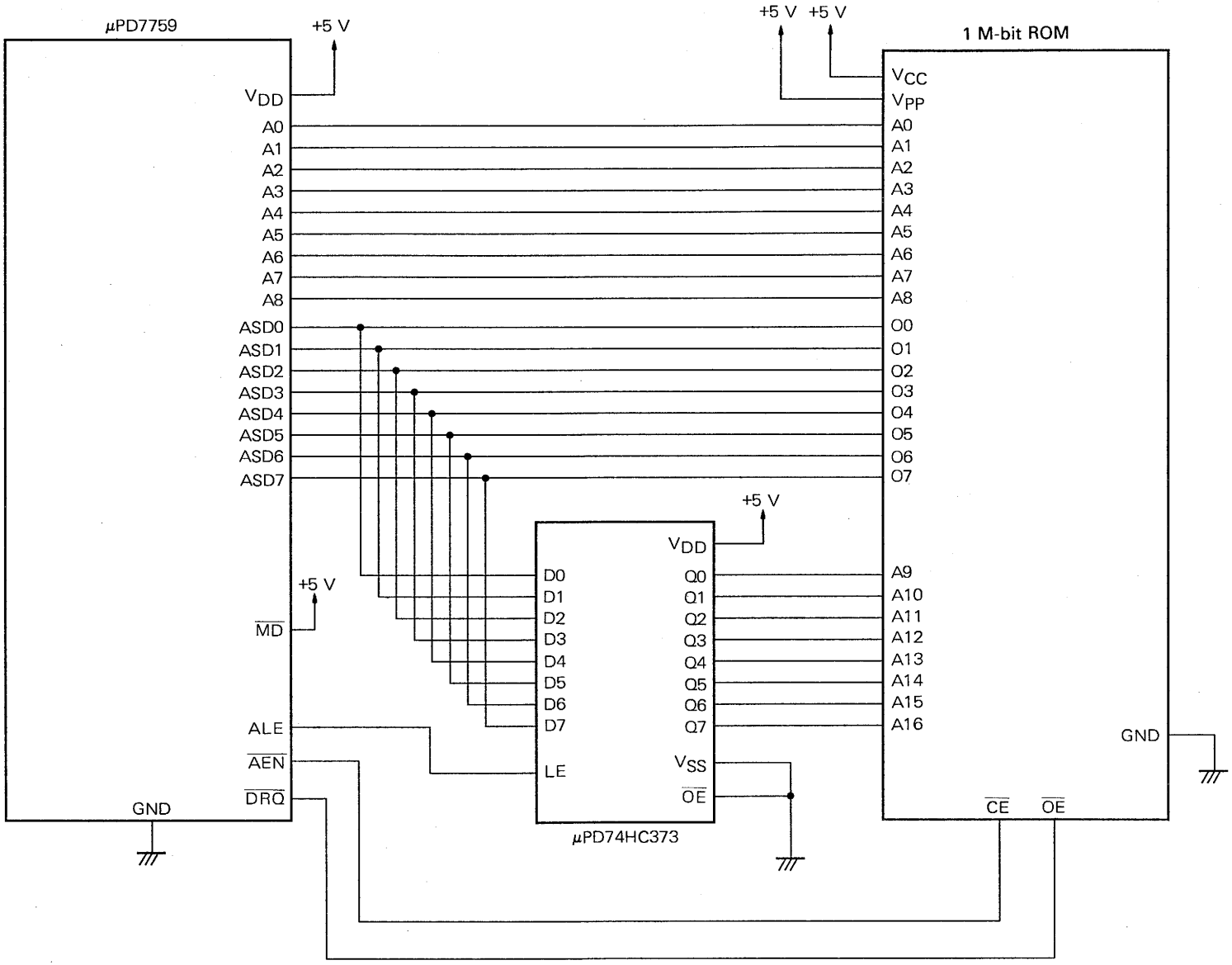
Using $\overline{BUSY}$ as an interrupt signal to the CPU is suitable where messages are frequently connected, whereas port sensing by the CPU as necessary is suitable where messages have a relatively simple structure, with the CPU's emphasis placed on other processing.

4.1.3 External ROM connection (μPD7759)

An 8-bit/word memory is best recommended for external connection to the μPD7759. Its access time should be up to 6 μs.

Fig. 4-5 shows the interface with the 1 M-bit ROM

Fig. 4-5 Interfacing with the 1 M-bit ROM



4.2 Low-Pass Filter

Digitized signals contain not only the original signal but also Loopback signals generated from harmonics of the sampling frequency as a loopback frequency.

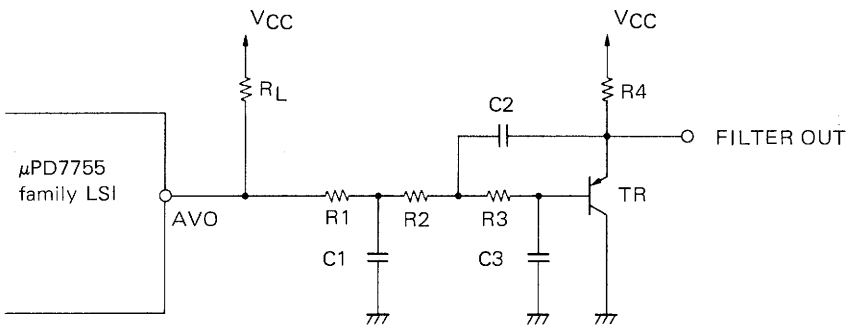
To reproduce only the original signal, frequencies above one half of the sampling frequency must be cut off. A filter with as sharp a cutoff slope as possible is desirable for this purpose. For audio signals, a cutoff slope of −48 dB/oct or more is ideal. In practice, however, the filter circuit can be simplified depending on the reproduction performance or other characteristics of the speaker used. Two examples of typical low-pass filters are shown below, one using a transistor and one using an operational amplifier.

4.2.1 Low-pass filter using a transistor

(1) Circuit and its operation

Fig. 4-6 shows a −18 dB/oct low-pass filter organized of a single PNP transistor. The transistor is configured as an emitter-follower connection, and the analog output voltage of a μPD7755 family LSI is used as its base bias. As a result, the transistor is normally biased only when audio signals are output from the μPD7755 family LSI. In all other instances, the transistor is not biased at all, with a power consumption of 0.

Fig. 4-6 Typical low-pass filter circuit (using transistor)



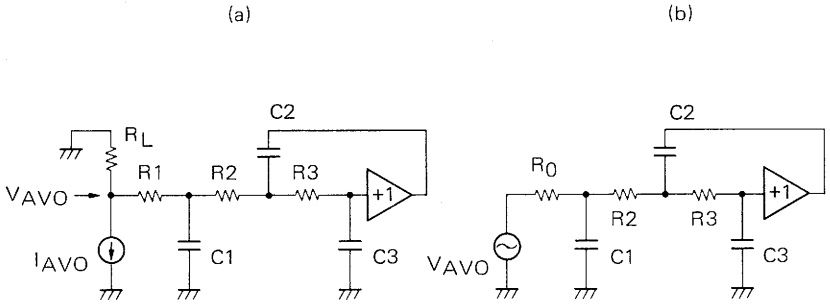
C1: 0.047 μF
C2: 0.1 μF
C3: 0.0068 μF

$R1 + R_L = R2 = R3$
R4 = 510 Ω
TR: 2SA733, etc.

(2) Cutoff frequency setting

Fig. 4-7 (a) is an AC equivalent circuit of the low-pass filter shown in Fig. 4-6. Fig. 4-7 (b) is a modification to the circuit to have a voltage source as the signal source. Apparently, the load resistor R_L connected to the AVO pin of the μPD7755 family LSI forms part of the circuit constant of the low-pass filter.

Fig. 4-7 AC equivalent circuit (using transistor)

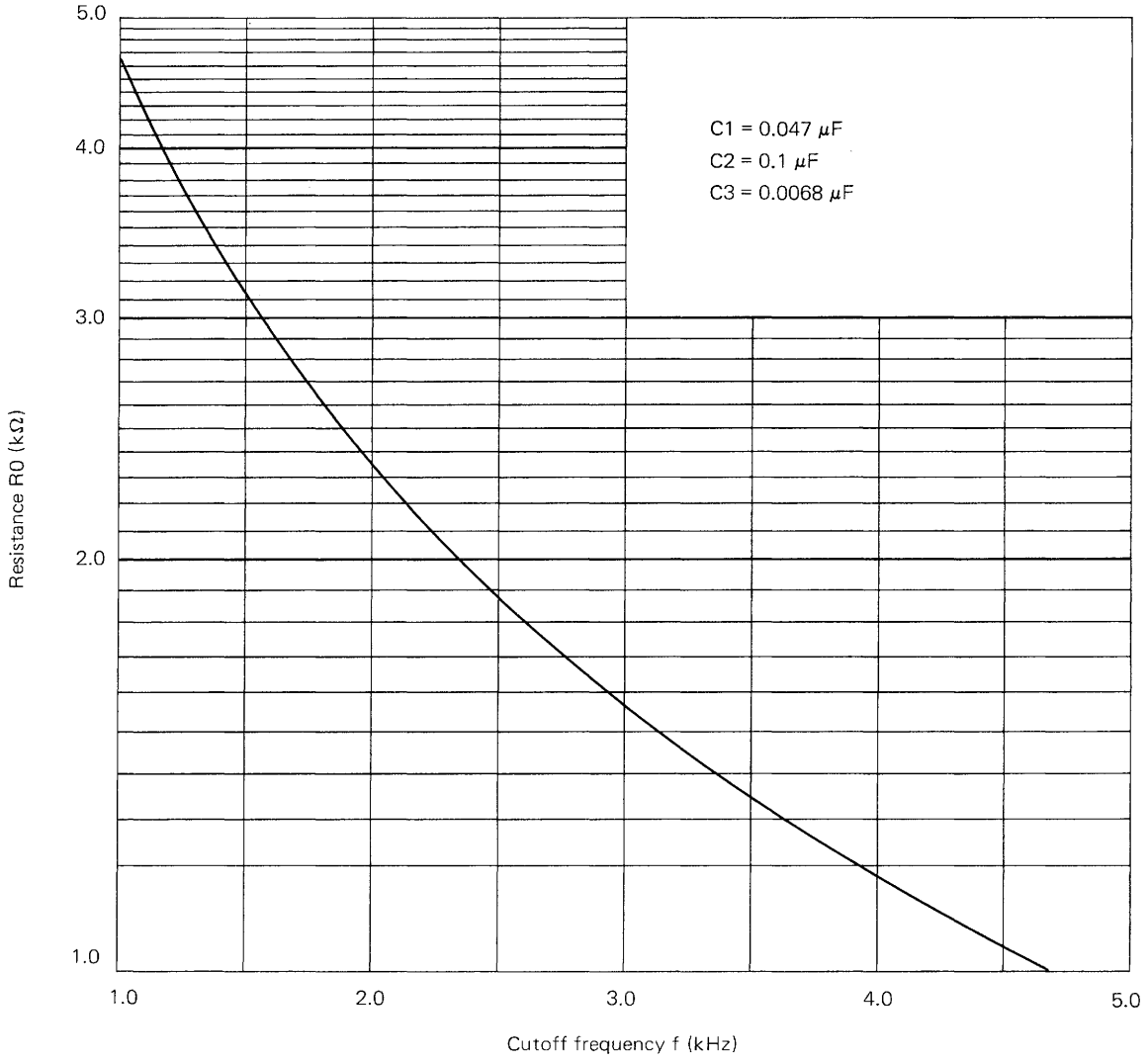


For the low-pass filter shown in Fig. 4-6, the cutoff frequency can be easily altered by changing R_L and R1 to R3 with C1 to C3 being fixed.

Fig. 4-8 gives the relationship between these resistances and the cutoff frequency. R0 in the figure is expressed as

$$R0 = R1 + R_L$$
$$= R2$$
$$= R3$$

Fig. 4-8 Low-pass filter resistance constants (using transistors)



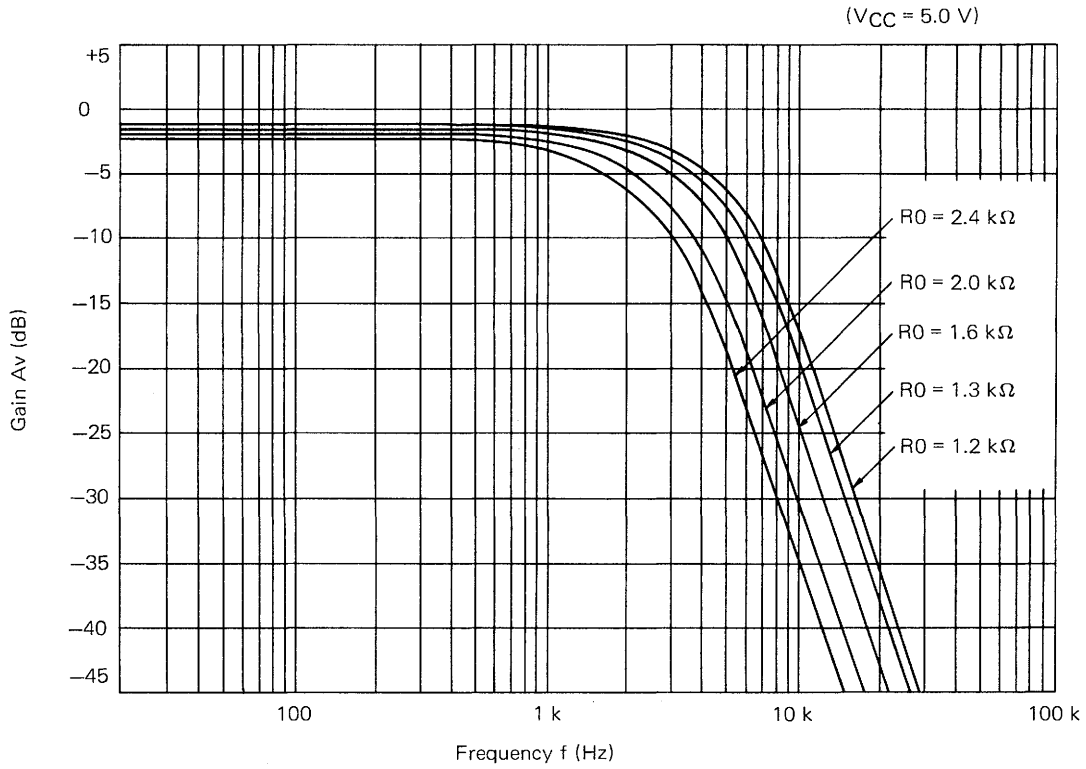
With a sampling frequency of 6 kHz, for example, a cutoff frequency of about 2.4 kHz is appropriate for the low-pass filter.

The resistance R0 corresponding to the cutoff frequency of 2.4 kHz is found to be 2 kΩ in Fig. 4-8. If 390 Ω is used as the load resistor R_L in the μPD7755 family LSI, the resistances will be:

R1 = 1.6 kΩ (R_L = 390 Ω)
R2 = 2.0 kΩ
R3 = 2.0 kΩ

Fig. 4-9 gives measurements of the frequency response obtained by varying R0 from 1.2 kΩ to 2.4 kΩ.

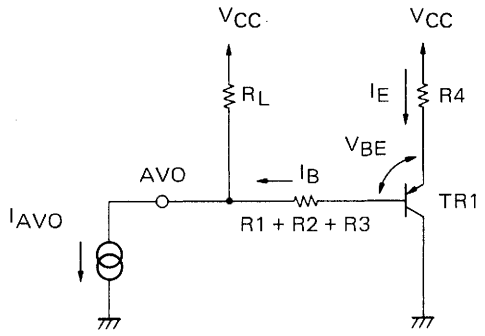
Fig. 4-9 Gain vs. frequency response (Measured data: using transistors)



(3) DC bias voltage level setting

The DC equivalent circuit shown in Fig. 4-6 can be represented as in Fig. 4-10.

Fig. 4-10 DC equivalent circuit



The emitter-follower circuit of TR1 functions normally only if its base voltage level V_B meets the equation

$$V_B < V_{CC} - I_E \cdot R_4 - V_{BE} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

With I_E = 3 mA and R_4 = 510 Ω, for example, the base voltage level is given from $V_{BE} \fallingdotseq 0.7$ Vas

$$V_B = V_{CC} - 2.23 \quad \ldots\ldots (2)$$

If the voltage level of the AVO pin of the μPD7755 family LSI is V_{AVO} and the base current in TR1 is I_B, V_{AVO} is stated as

$$V_{AVO} = V_B - I_B \cdot (R1 + R2 + R3) \quad \ldots\ldots (3)$$

Since, generally, I_B is about one hundredth of I_E and R1 is on the order of several kΩ, V_{AVO} can be expressed as

$$V_{AVO} \fallingdotseq V_{CC} - 2.3 \quad \ldots\ldots (4)$$

Namely, the AVO pin voltage must be at least 2.3 V lower than V_{CC} while audio signals are being output from the μPD7755 family LSI.

This setting is effected by adjusting the reference current in the μPD7755 family LSI or adjusting the load resistor R_L.

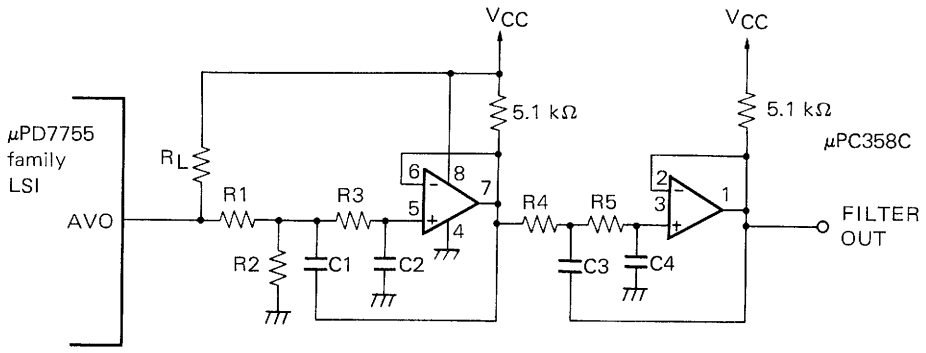
4.2.2 Low-pass filter using an operational amplifier

(1) Circuit and its operation

Fig. 4-11 shows a −24 dB/oct low-pass filter organized of a dual operational amplifier μPC358C. The operational amplifier is configured as a voltage follower connection, and the analog output voltage of a μPD7755 family LSI is used as its bias.

Since the μPC358C has an in-phase input voltage range of 0 to V_{CC} −1.5 V, the analog output voltage of the μPD7755 family LSI is divided by the resistors R1 and R2 before it is input to the filter circuit.

Fig. 4-11 Typical low-pass filter circuit (using operational amplifier)

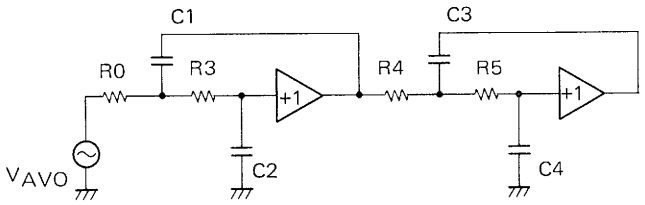


C1: 0.022 μF
C2: 0.0022 μF
C3: 0.022 μF
C4: 0.01 μF
R_L: 510 Ω

(2) Cutoff frequency setting

Fig. 4-12 is an AC equivalent circuit of the low-pass filter shown in Fig. 4-11.

Fig. 4-12 AC equivalent circuit (using operational amplifier)



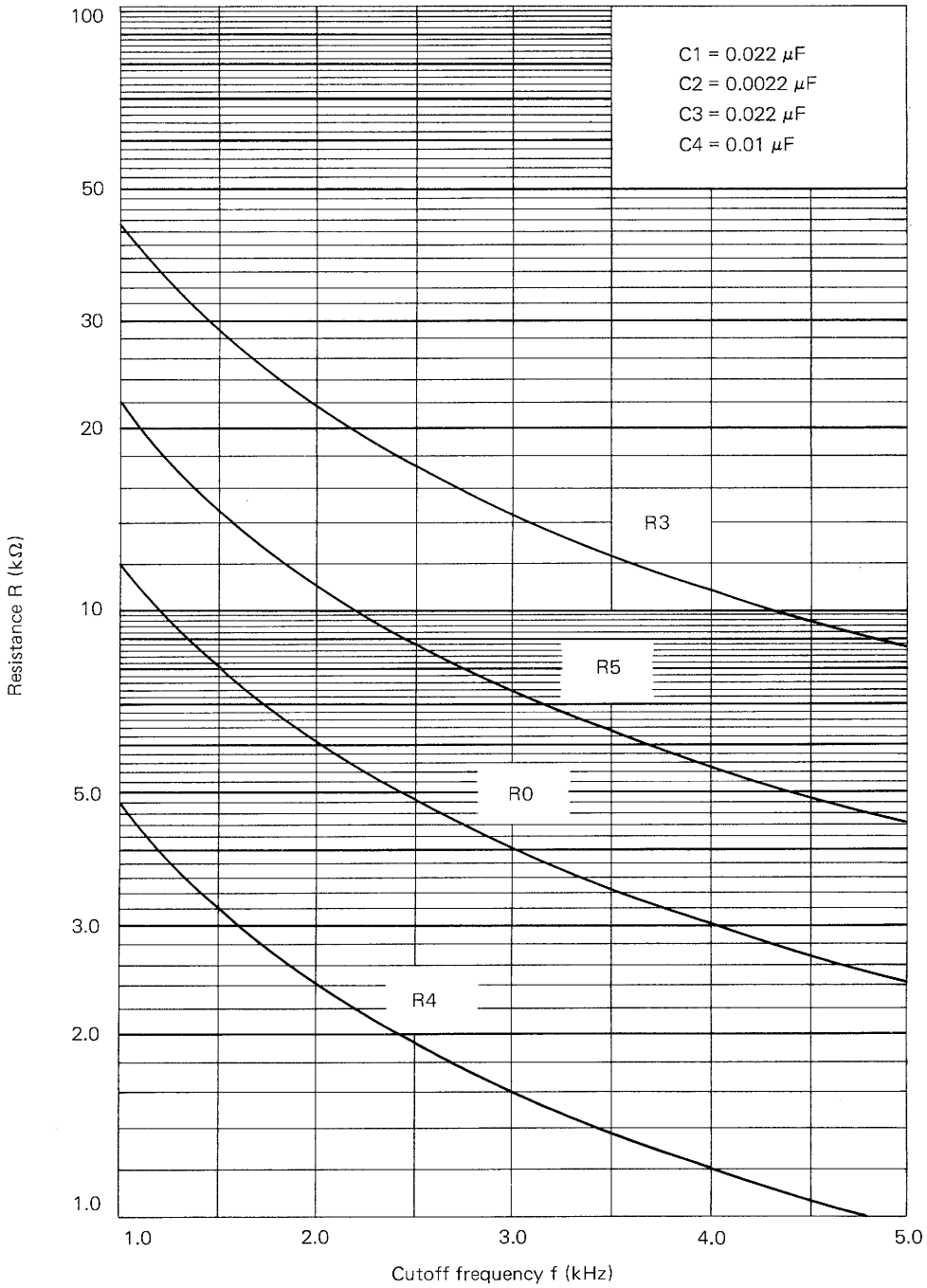
R0 in the figure is a combined resistance of the load resistor R_L in the μPD7755 family LSI and R1 and R2 in the circuit diagram. It is expressed as

$$R0 = \frac{(R_L + R1)\, R2}{R_L + R1 + R2} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (5)$$

For the low-pass filter shown in Fig. 4-11, the cutoff frequency can be easily altered by changing R_L and R1 to R5 with C1 to C4 being fixed.

Fig. 4-13 gives the relationship between these resistances and the cutoff frequency. R0 in the figure is a combined resistance expressed by Equation (5).

Fig. 4-13 Low-pass filter resistance constants (using operational amplifier)



The procedure for selecting circuit constants is described below with reference to a sampling frequency (fs) of 8 kHz. With a sampling frequency of 8 kHz, a cutoff frequency of about 2.4 kHz is appropriate for the low-pass filter.

On the basis of Fig. 4-13, the resistances at fc = 3.6 kHz will be:

R0 ≒ 3.3 kΩ
R1 ≒ 1.2 kΩ
R2 ≒ 1.3 kΩ
R3 ≒ 6.2 kΩ

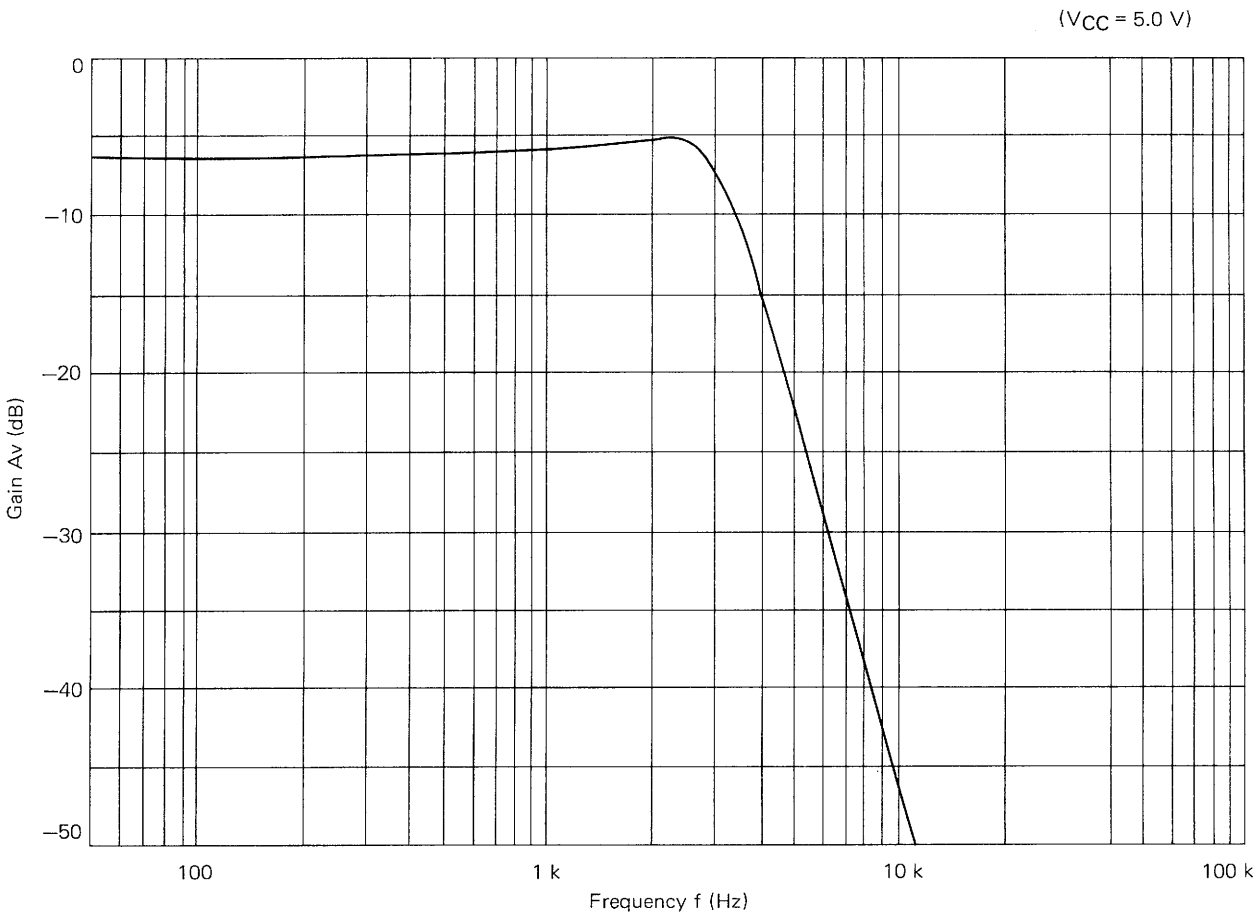
Next, the values of R1 and R2 in the circuit diagram are calculated from R0. If R1 = R2 = R is assumed for simplicity's sake, Equation (5) can be transformed as follows.

$$R^2 + R\,(R_L - 2 \cdot R0) - R0 \cdot R_L = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

By assigning $R_L = 510\ \Omega$ and $R0 = 3.3\ k\Omega$ to this equation, one obtains $R \fallingdotseq 6.4\ k\Omega$. Namely, the resistances in the circuit diagram will be:

R1 = 6.4 kΩ
R2 = 6.4 kΩ
R3 = 1.2 kΩ
R4 = 1.3 kΩ
R5 = 6.2 kΩ
R_L = 510 Ω

Fig. 4-14 Gain vs. frequency response (Measured data: using operational amplifier)



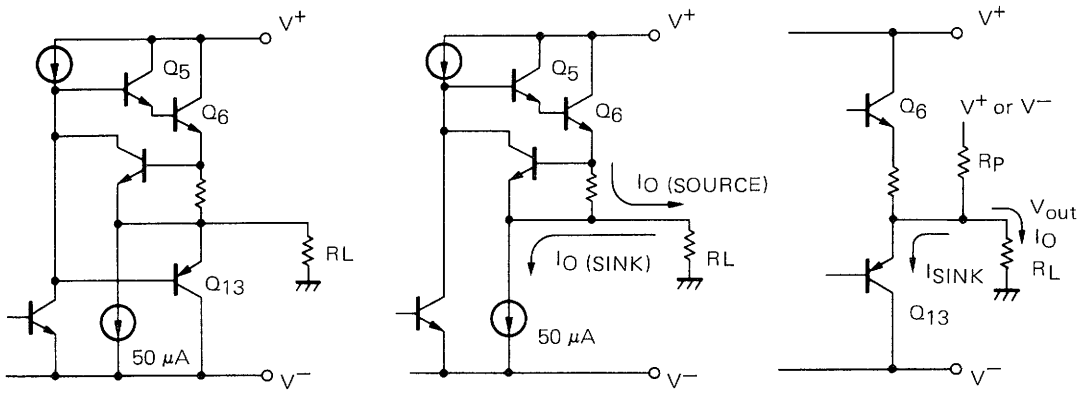
μPC358C is a dual operational amplifier operating at a single supply voltage of 3 V or higher. It is ideal for use in low-pass filters in μPD7755 family LSIs.

However, μPC358C was originally designed as a DC amplifier, and certain care should be observed when it is used to amplify AC signals in low-pass filters or similar devices.

Fig. 4-15 (a) shows an output-stage equivalent circuit of μPC358C, which is composed of a class C push-pull circuit. During current drainage, the output circuit is switched to suit the current as shown in Fig. 4-15 (b), generating crossover distortion during switching times.

The crossover distortion can be lessened by running the transistors, Q5, Q6, or Q13, in the output stage as emitter-followers (class A operation). This is accomplished by connecting a pull-up or pull-down resistor.

Fig. 4-15 Output-stage equivalent circuit of the μPC358C



(a) Output-stage equivalent circuit

(b) Output circuit operation when $I_O < 50\ \mu A$

(c) Effect of pull-up resistor

4.2.3 Typical LC filter circuit

Fig. 4-16 shows a typical LC filter circuit. Since the coil used has a terminal resistance of 270 Ω, the analog output load resistor of the μPD7755 family LSI is set to 270 Ω. Fig. 4-17 shows the frequency response of this circuit.

Fig. 4-16 Typical LC filter circuit

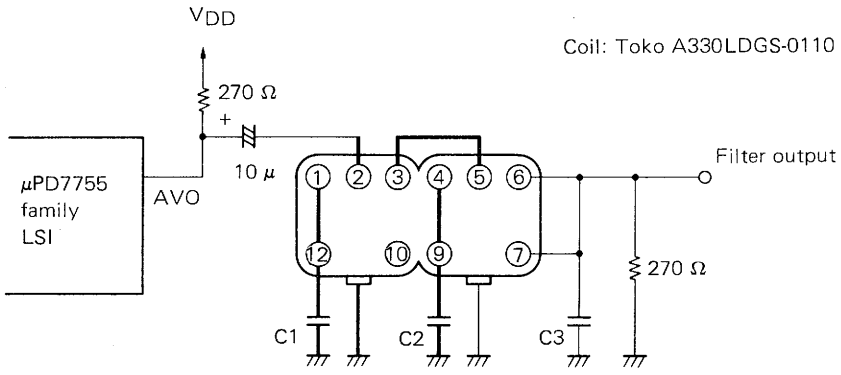
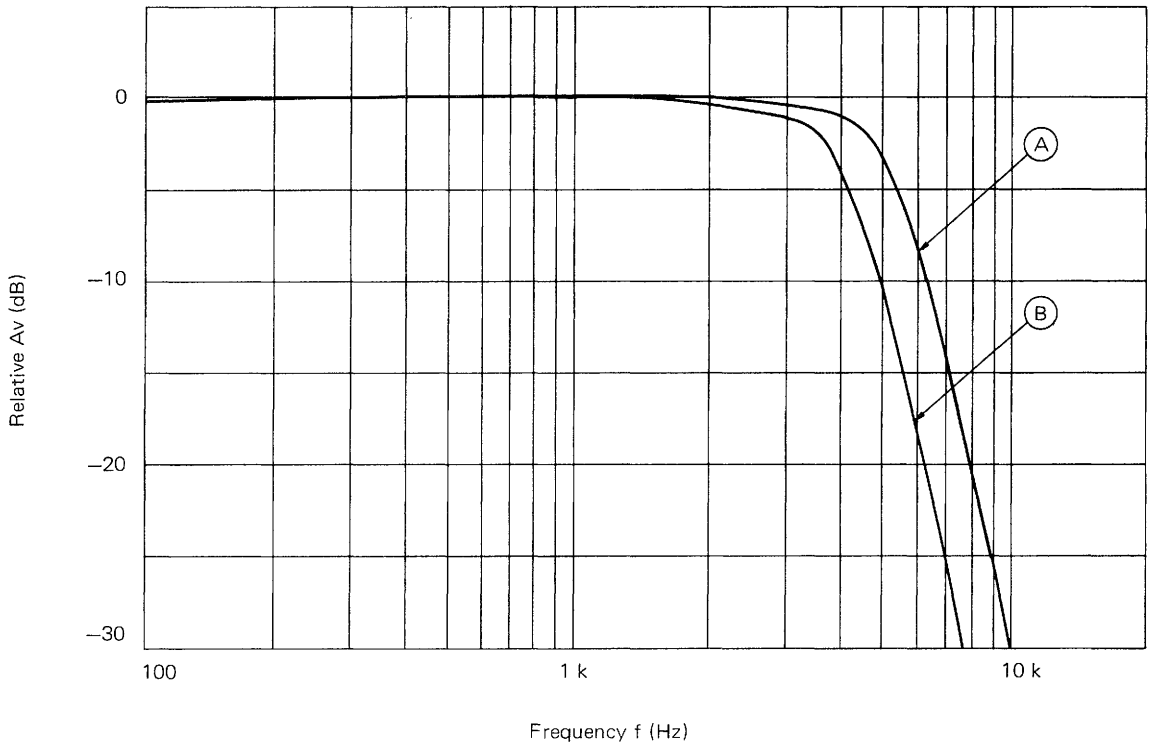


Fig. 4-17 Gain vs. frequency response (Measured data: using LC filter)



	A	B	Unit
C1	0.12	0.22	μF
C2	0.22	0.39	
C3	0.12	0.12	

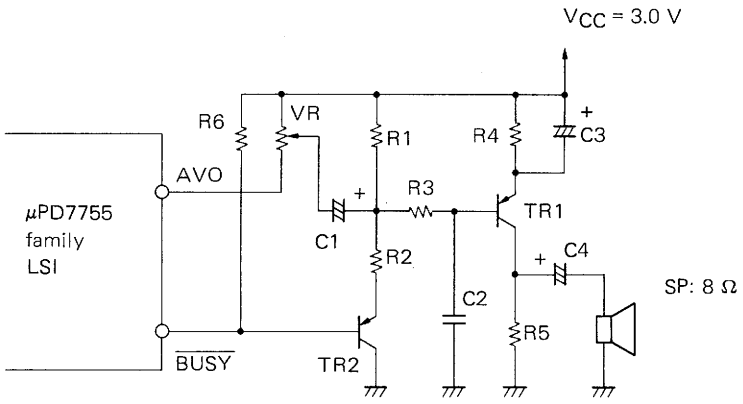
4.3 Speaker Amplifier

4.3.1 Speaker amplifier using transistors

Fig. 4-18 shows a typical speaker amplifier made up of transistors. With a standby function and a simple filtering function, the amplifier outputs about 20 mW at V_{CC} = 3 V.

The circuit is composed of TR1 that drives the speaker through class A operation, and TR2 that turns on and off the DC bias for TR1 according to the BUSY signal in the μPD7755 family LSI. C1 and C3 form a high-pass filter, R3 and C2, a low-pass filter.

Fig. 4-18 Typical speaker amplifier using transistors

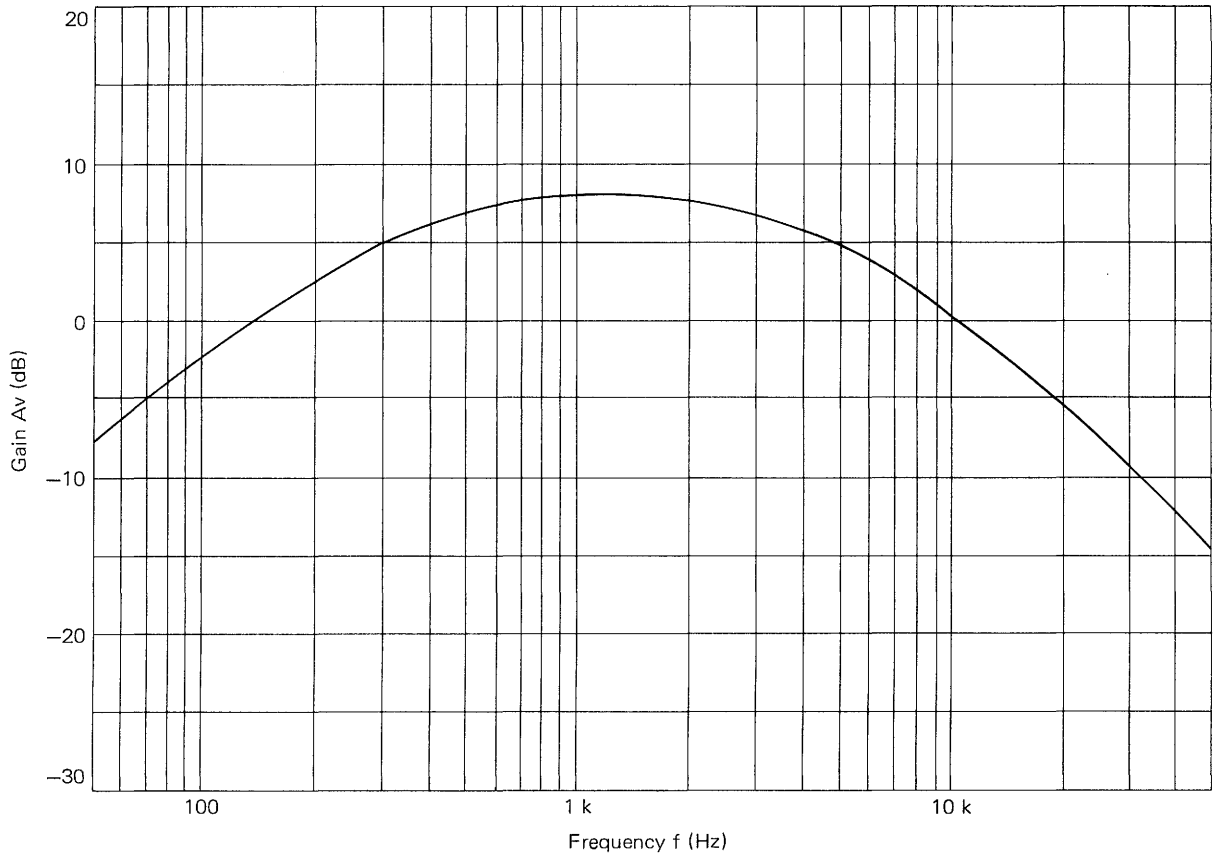


TR1: 2SA733
TR2: 2SA733

Part number	Constant
VR	100 Ω
R1	470 Ω
R2	560 Ω
R3	220 Ω
R4	3 Ω
R5	8.2 Ω
R6	30 kΩ
C1	33 μF
C2	0.47 μF
C3	470 μF
C4	100 μF

Fig. 4-19 shows the gain vs. frequency response of this circuit.

Fig. 4-19 Gain vs. frequency response (Measured data: using speaker amplifier)

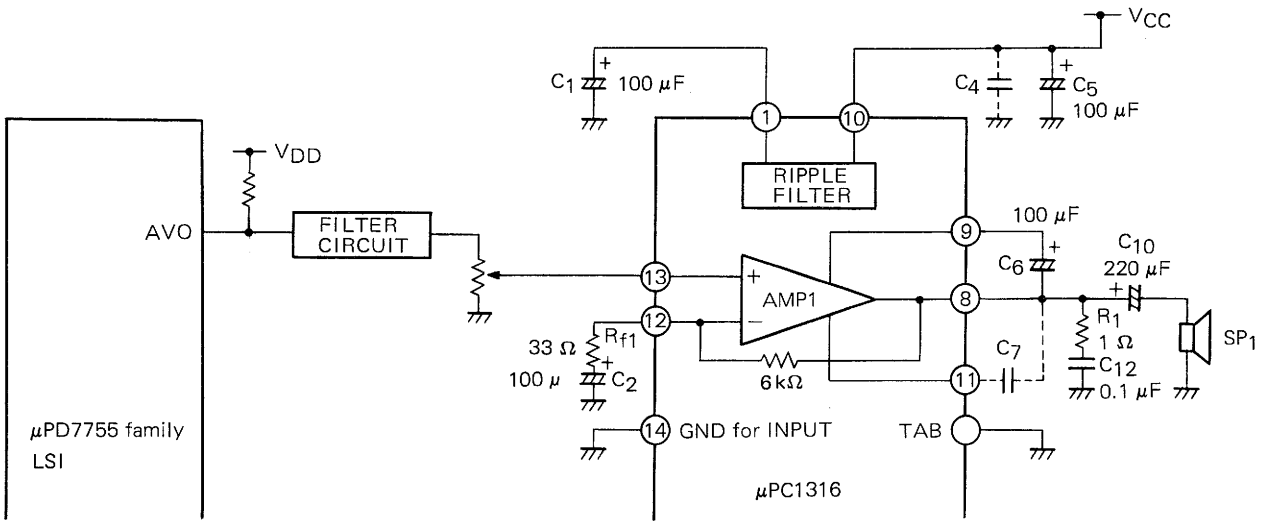


★ **4.3.2 Typical configuration using μPC1316**

Fig. 4-20 shows a typical speaker amplifier using μPC1316.

Given a supply voltage of 5.0 V, μPC1316 can output about 0.7 W (T.H.D. = 10 %) using a 4 Ω speaker.

Fig. 4-20 Speaker amplifier using μPC1316[Note]



Note The pins 2 to 6 of the μPC1316 are not used. These are pins for AMP2.

Caution 1. Mylar capacitor is recommended as C_{12}.

2. Add C_7 in the case of reducing voltage gain at high frequency.

3. Add C_4 or increase capacitance of C_{12} when a oscillation may occur due to the pattern layout on PCB.

4. Voltage gain can be changed by value of R_{f1}. The voltage gain should be set more than 34 dB.

5. When a input capacitor is connected to the input terminal, a bias resistor should be connected between the input terminal and GND.

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